

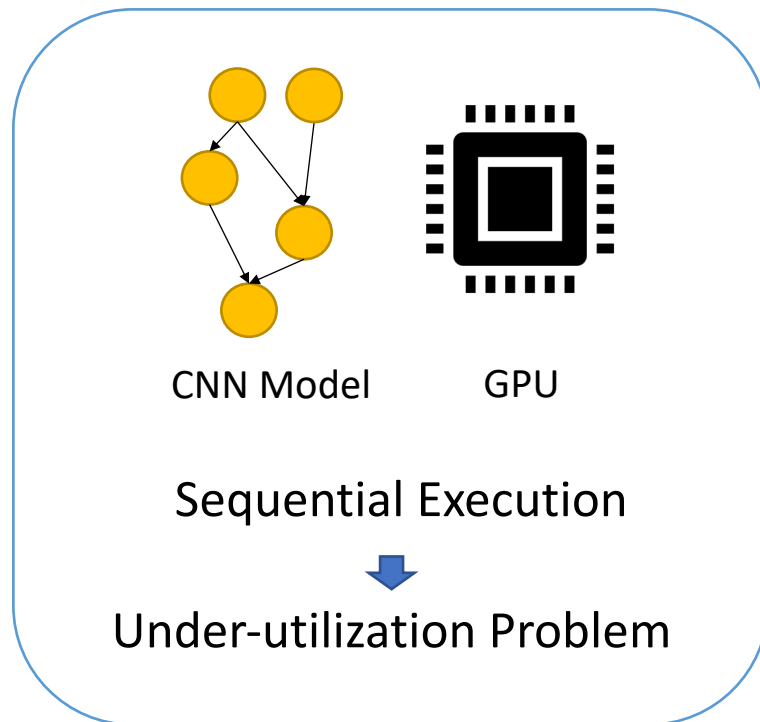
# IOS: Inter-Operator Scheduler for CNN Acceleration

Yaoyao Ding<sup>1 2</sup>, Ligeng Zhu<sup>3</sup>, Zhihao Jia<sup>4</sup>,  
Gennady Pekhimenko<sup>1 2</sup>, Song Han<sup>3</sup>

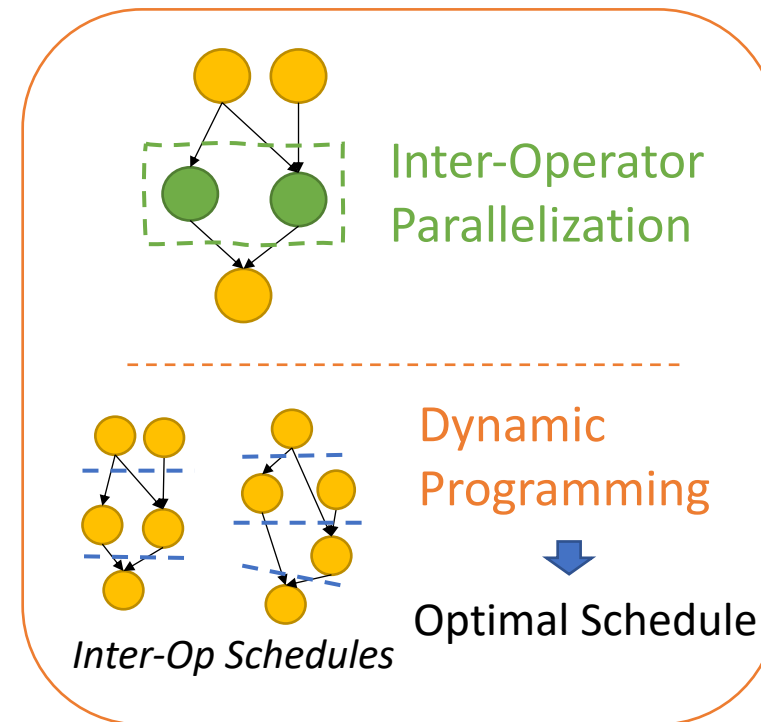


# Executive Summary

## Motivation

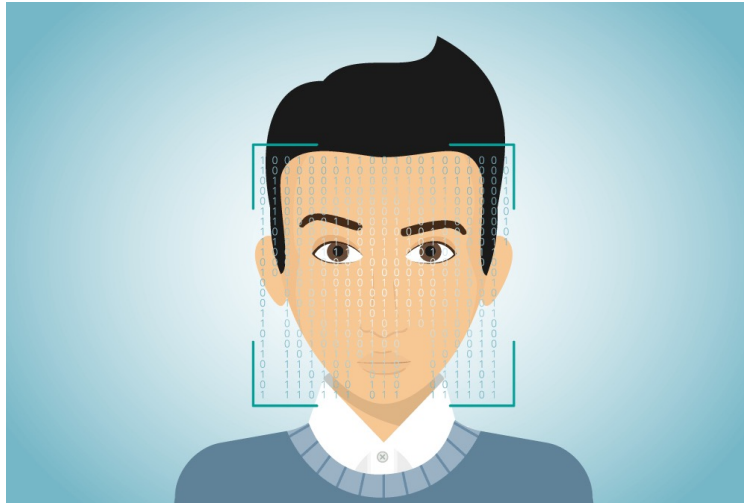


## Inter-Operator Scheduler

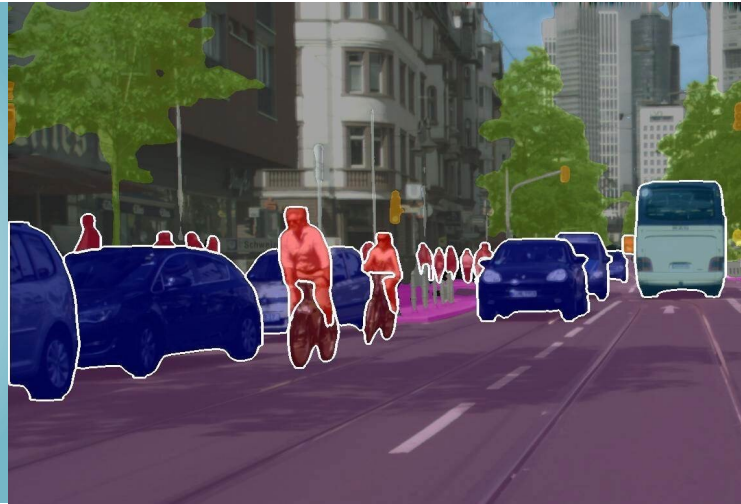


**1.1-1.5x speedup**

# Efficient Deployment of CNNs is Important



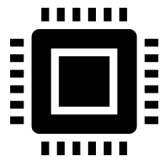
Face Recognition



Self Driving



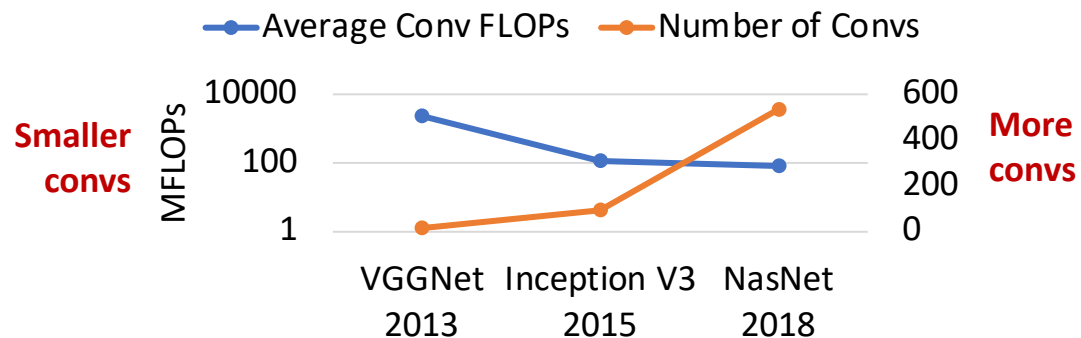
Language Translation



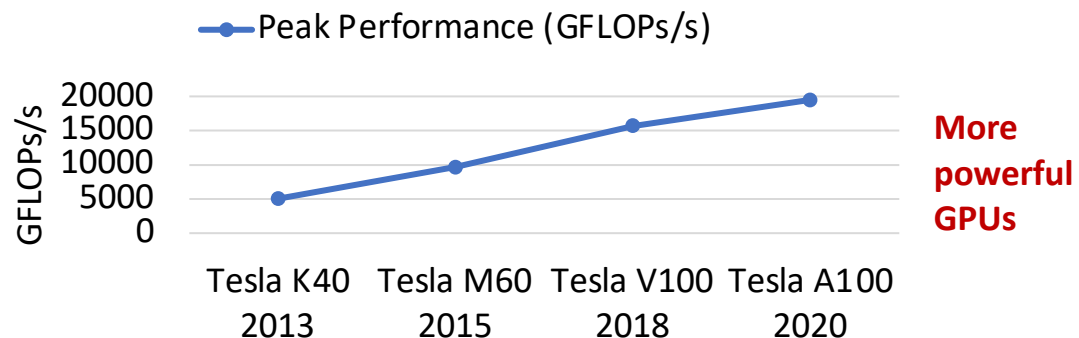
Is CNN inference in current DL libraries well utilizing underlying hardware?

# Motivation for Inter-Operator Parallelization

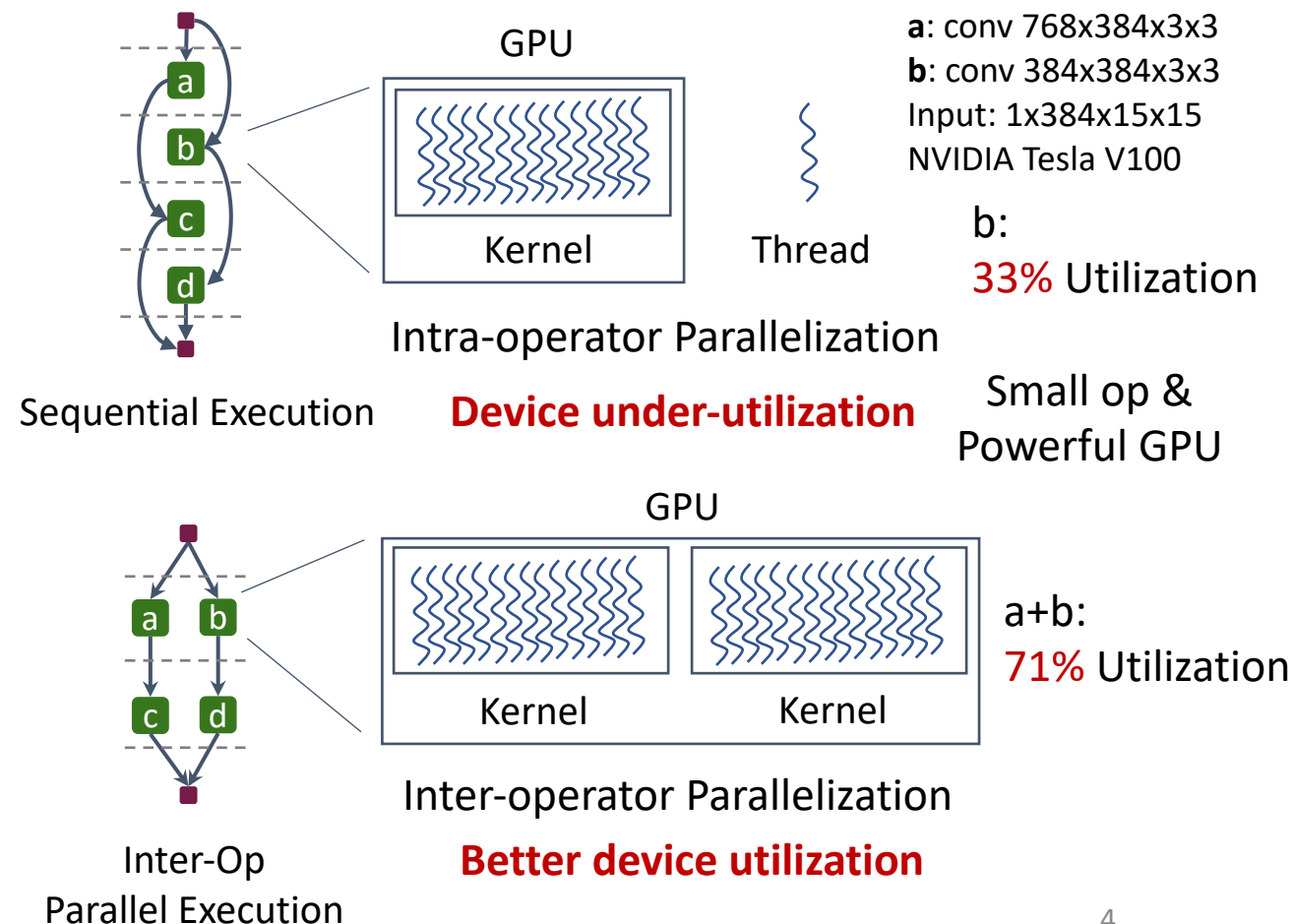
## 1. More small convs in CNN design.



## 2. GPU peak performance increased

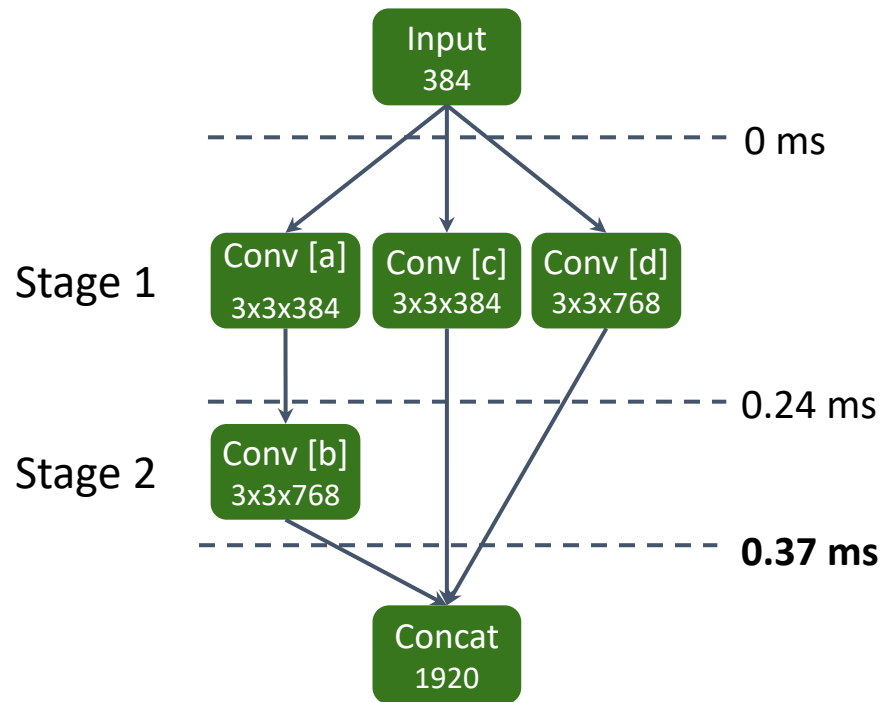


## 3. Intra- and Inter-operator Parallelization



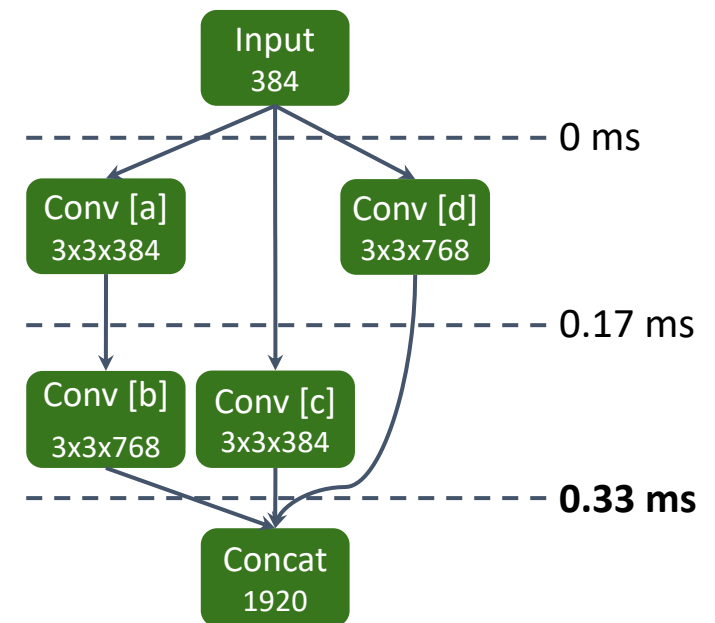
# Background: Wavefront Schedule Policy

Wavefront Schedule Policy: Execute **all available** operators stage by stage



Wavefront Schedule

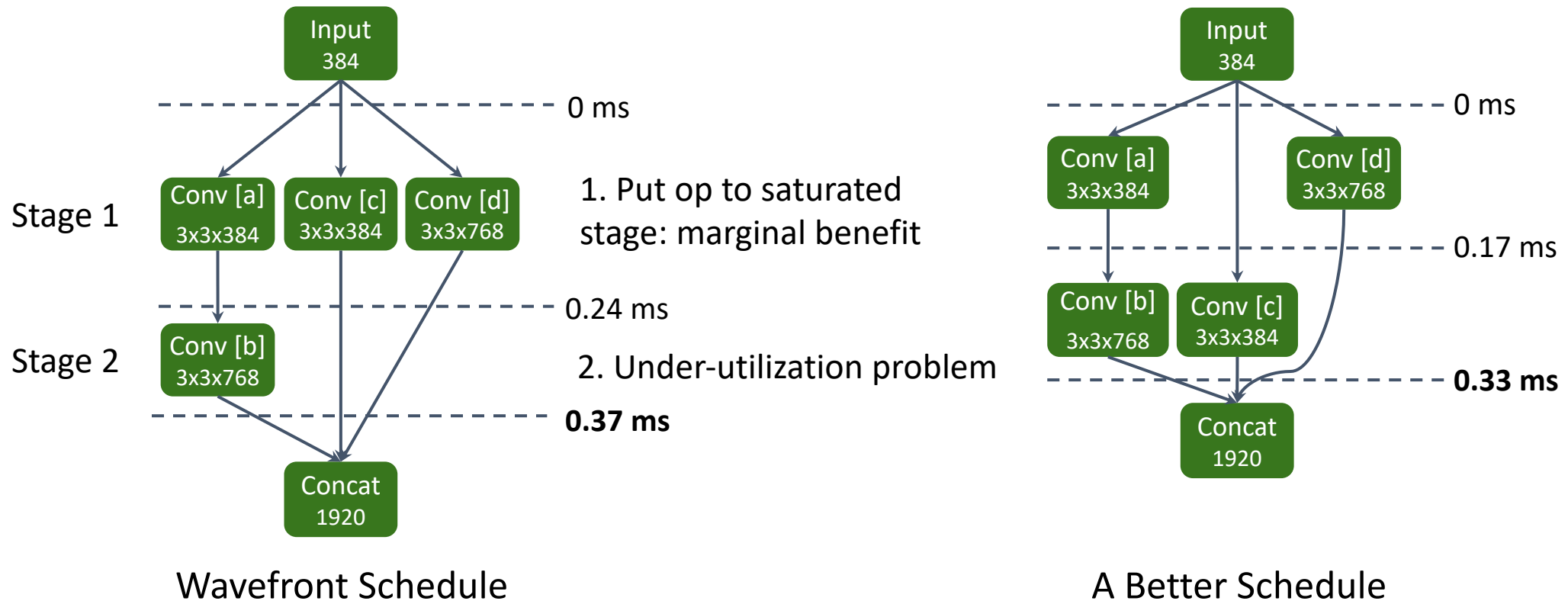
Move Conv [c] from Stage 1 to Stage 2



A Better Schedule

# Background: Wavefront Schedule Policy

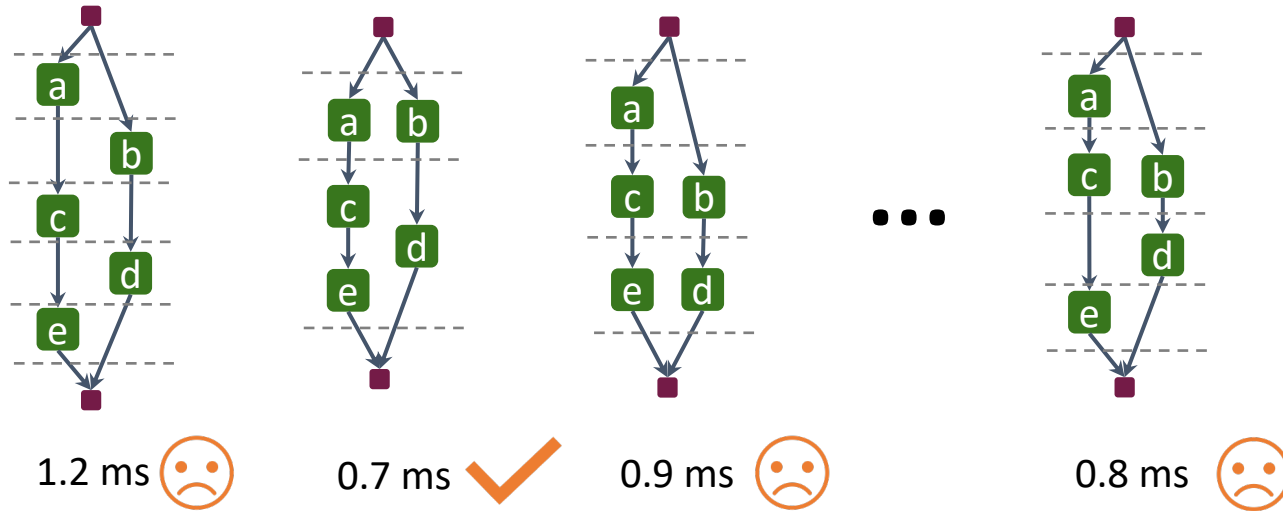
Wavefront Schedule Policy: Execute **all available** operators stage by stage



**Wavefront schedule policy is sub-optimal**

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**General Idea:** Explore the schedule space **exhaustively**.



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**Challenge:** The number of schedules is **exponential** in the number of operators.

e.g., NASNet has more than  $10^{12}$  schedules



**Prohibitive to enumerate**

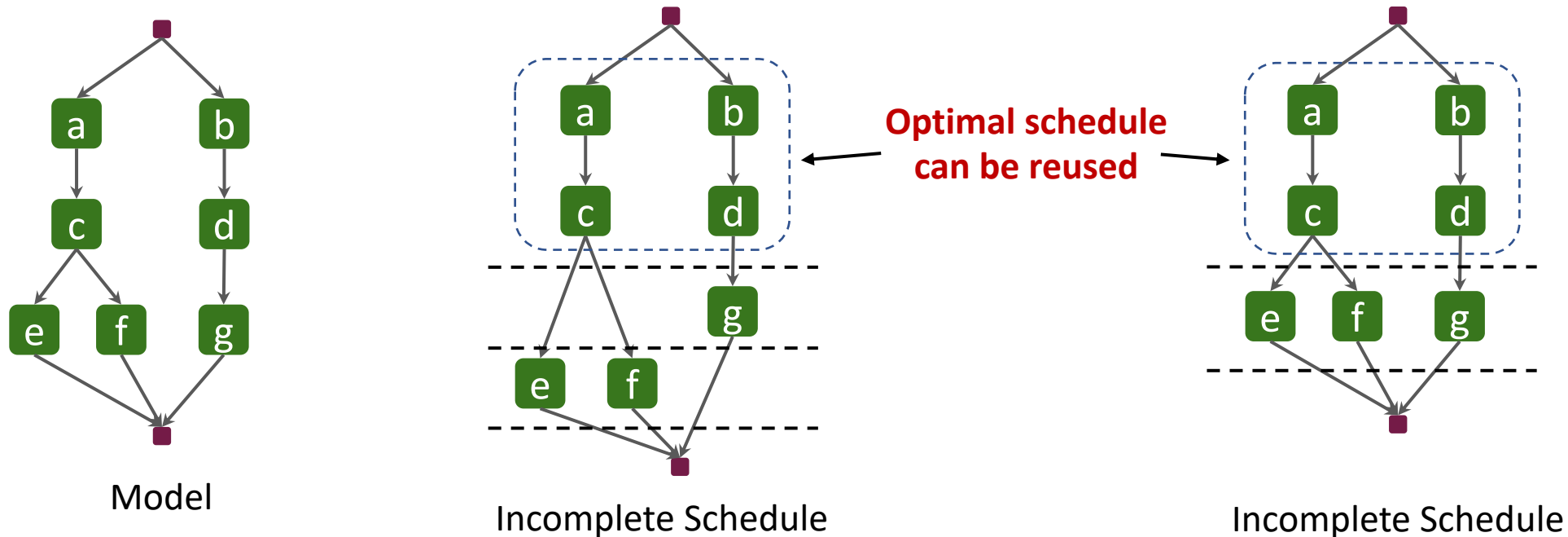


# Inter-Operator Scheduler (IOS)

**General Idea:** Explore the schedule space **exhaustively**.

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**Observation 1:** Optimal schedule for a subgraph can be reused



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**Key Idea:** Dynamic Programming

# Inter-Operator Scheduler (IOS)

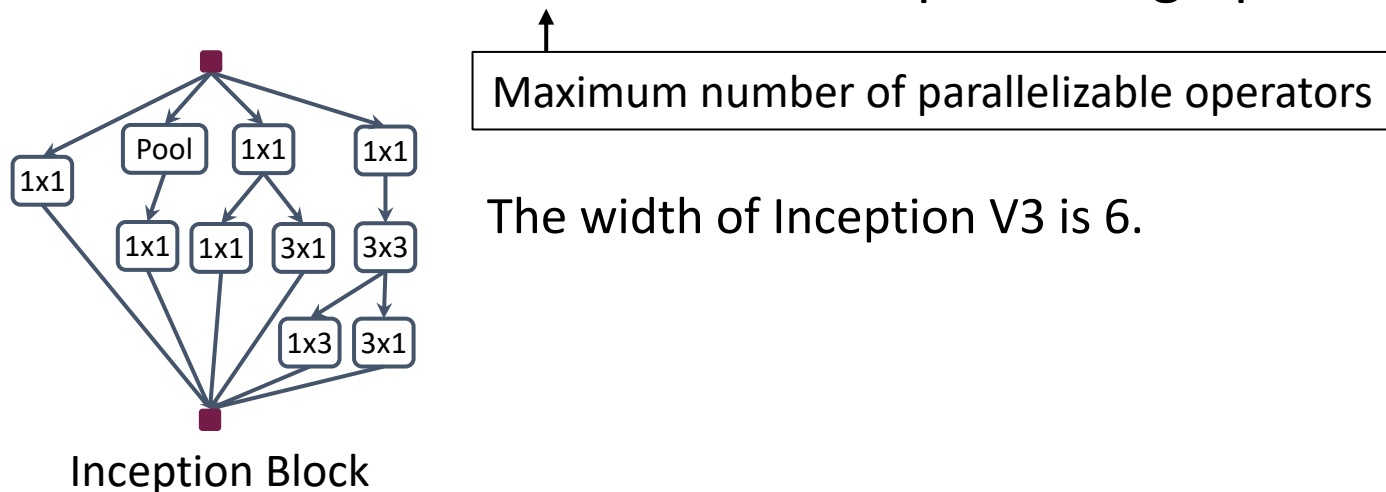
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**Key Idea:** Dynamic Programming

**Observation 2:** The width of the computation graph is usually small



# Inter-Operator Scheduler (IOS)

**General Idea:** Explore the schedule space **exhaustively**.

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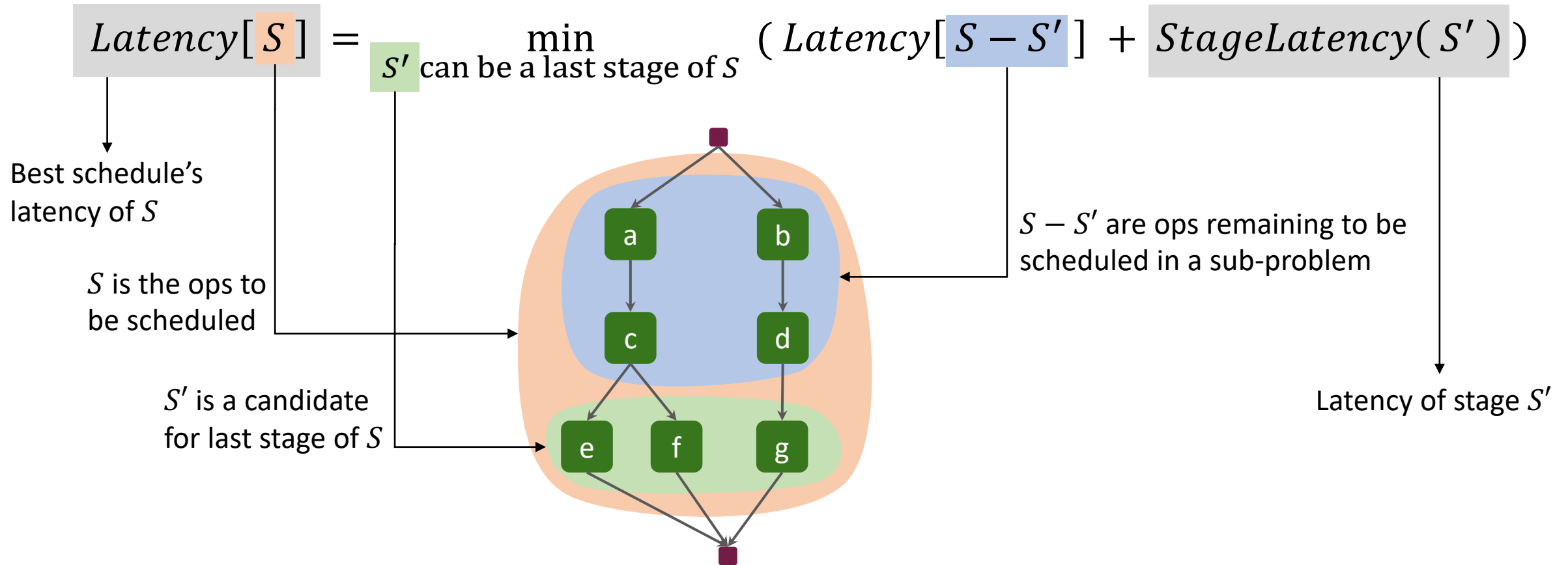
**Observation 1:** Optimal schedule for a subgraph can be reused

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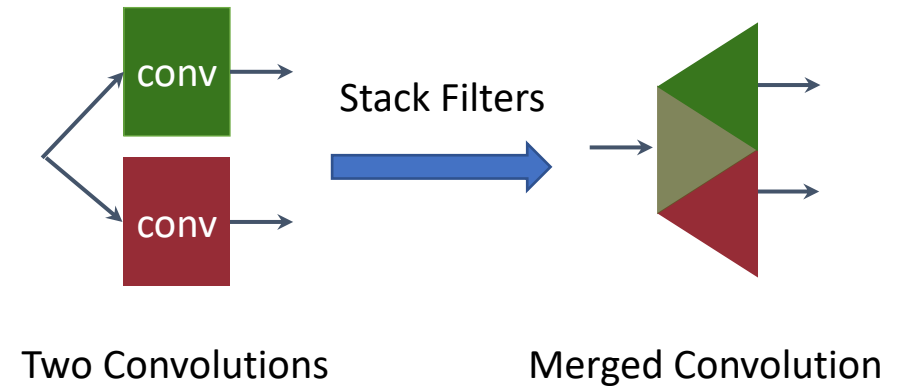
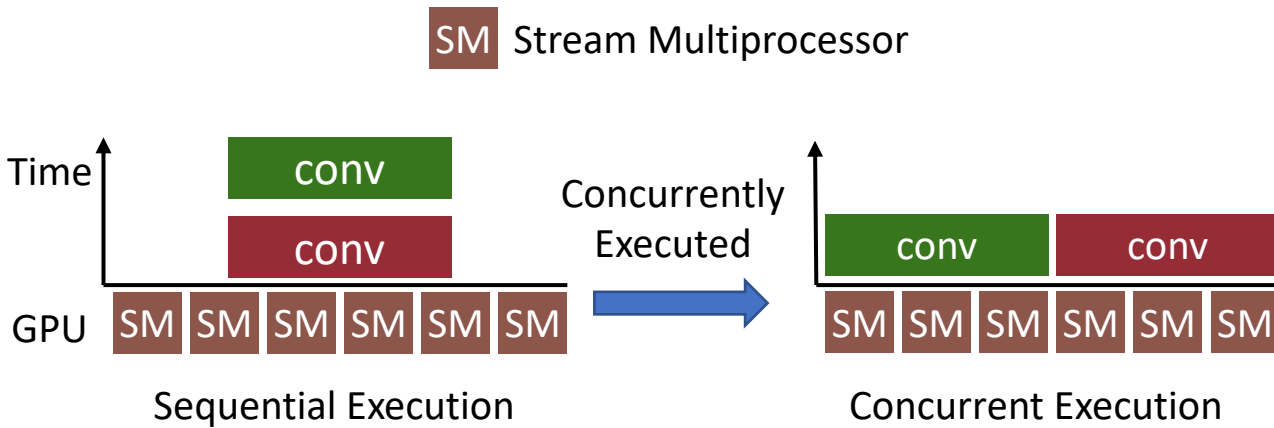
**Key Result:** Time complexity is only exponential in the width

# Inter-Operator Scheduler (IOS)



# Parallelization Strategy Selection

$$Latency[S] = \min_{S' \text{ can be a last stage of } S} ( Latency[S - S'] + StageLatency(S') )$$



Concurrent Execution

General  
Sub-optimal performance

## Profile & Select

Operator Merge

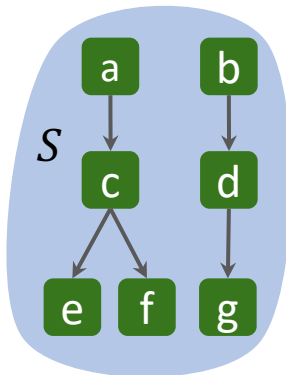
Specialized  
Usually better performance

# Last Stage Candidates

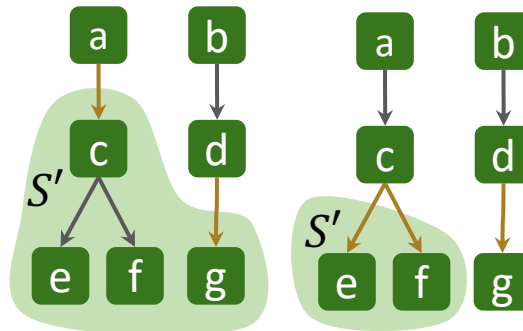
$$Latency[S] = \min_{S' \text{ can be a last stage of } S} ( Latency[S - S'] + StageLatency(S') )$$

$S'$  can be a last stage of  $S \iff$  There is no edge from  $S'$  to  $S - S'$

↓ Edge from  $S - S'$  to  $S'$

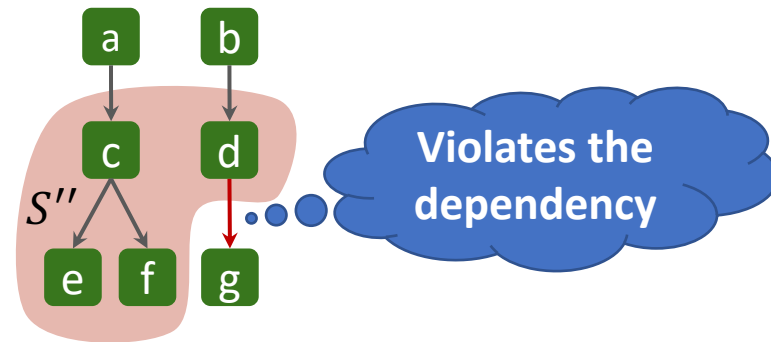


Operators  $S$  to be scheduled



$S'$  can be a last stage of  $S$

↓ Edge from  $S'$  to  $S - S'$



$S''$  can **NOT** be a last stage of  $S$

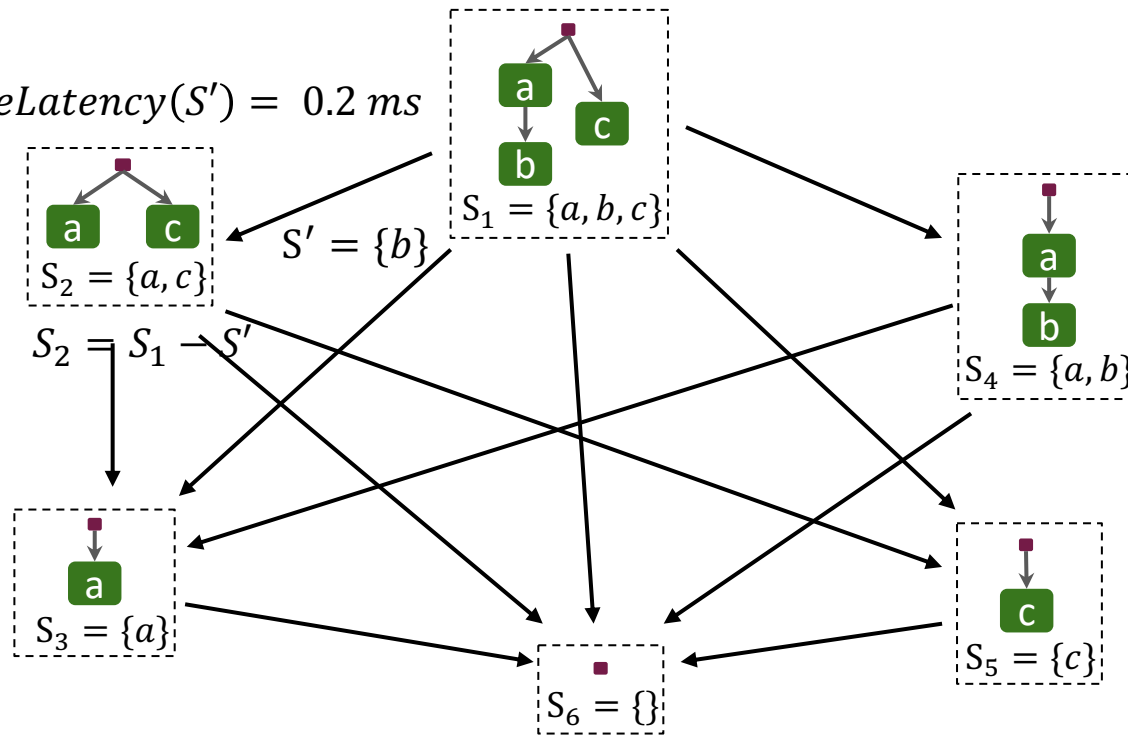
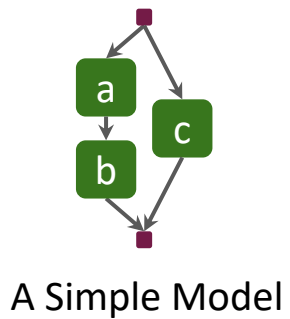
# Transition Graph and Time Complexity

$$Latency[S] = \min_{S' \text{ can be a last stage of } S} ( Latency[S - S'] + StageLatency(S') )$$

**Vertices:** all valid state  $S$

**Edges:**  $S \rightarrow (S - S')$

$StageLatency(S') = 0.2 \text{ ms}$



Transition Graph

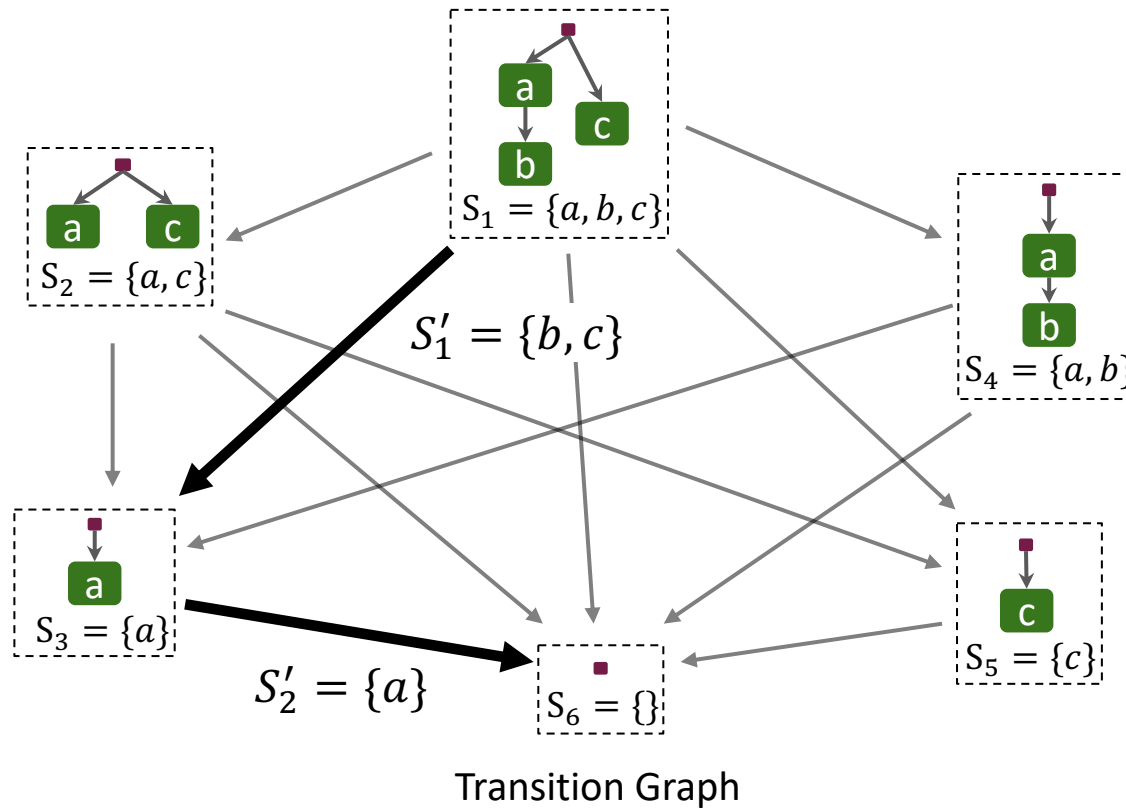
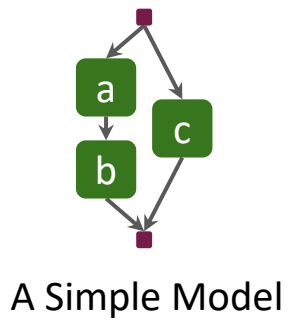


# Transition Graph and Time Complexity

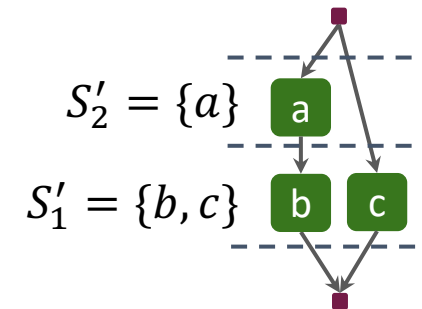
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IOS: Find the **shortest** path



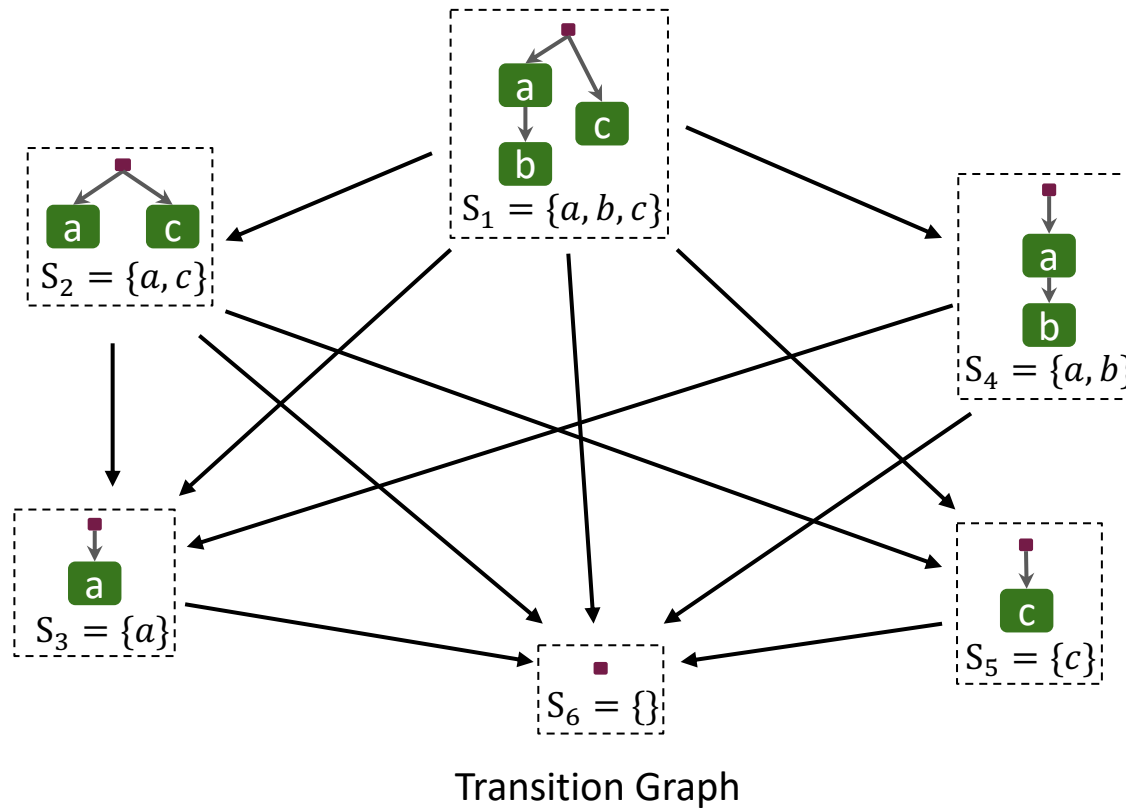
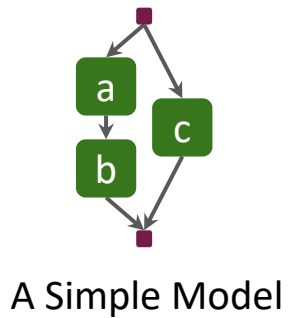
Any path from  $S_1$  to  $S_6$  is a schedule

# Transition Graph and Time Complexity

$$Latency[S] = \min_{S' \text{ can be a last stage of } S} ( Latency[S - S'] + StageLatency(S') )$$

**Vertices:** all valid state  $S$

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IOS: Find the **shortest** path

**Time Complexity** of IOS:

$$O\left(\left(\frac{n}{d} + 1\right)^{2d}\right)$$

**n:** number of operators

**d:** max number of parallelizable ops

# Methodology

- **Benchmarks**

- Inception V3
  - SqueezeNet
  - Randwire
  - NasNet
- } Expert Designed
- } Neural Architecture Search

- **Environment**



NVIDIA Tesla V100



10.2



7.6.5

- **Baselines**

- State-of-the-art Frameworks (cuDNN-based)



- Different schedules on IOS Runtime

- **IOS Implementation**

- cuDNN kernels
- CUDA Stream

# Comparison of cuDNN-based Frameworks

**Tensorflow:** A popular machine learning framework.

**Tensorflow-XLA:** TensorFlow with compilation optimization.

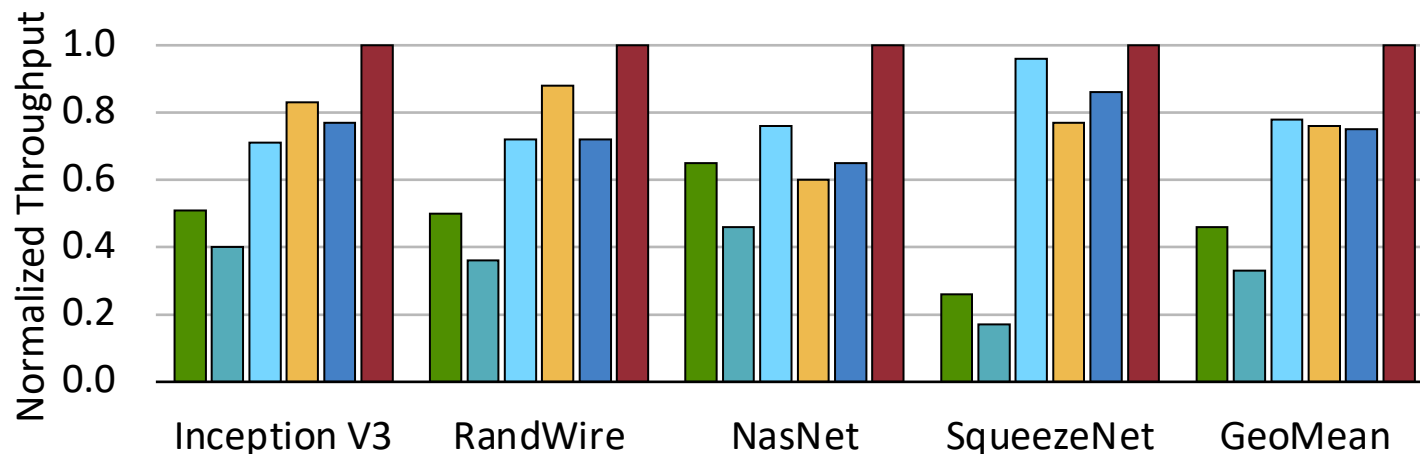
**TASO:** Transformation-based optimizer.

**TVM-cuDNN:** TVM backed with cuDNN convolution kernel.

**TensorRT:** NVIDIA high-performance inference engine.

**IOS:** Our method

Under-utilization due to sequential execution



**IOS** outperforms all frameworks and achieves **1.1-1.5x** speedup.

Performance is normalized to the best framework

# Comparison of Different Schedules

Under-utilize Device

**Sequential:** Run each op sequentially.

**Wavefront:** Run all available ops stage by stage.

**IOS-Merge:** IOS with only “operator merge” policy.

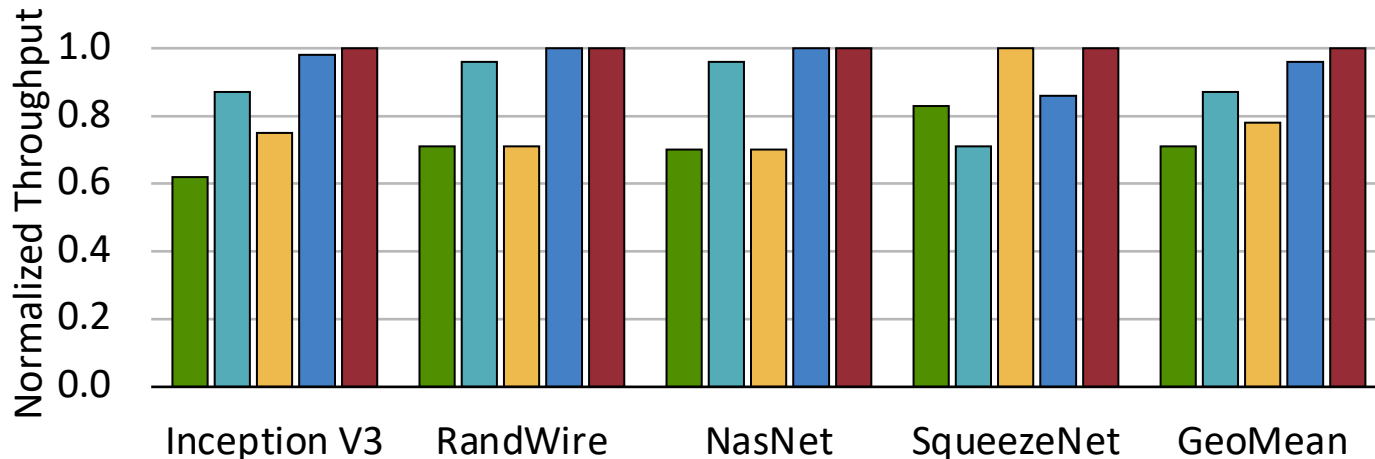
**IOS-Parallel:** IOS with only “parallel execution” policy.

**IOS-Both:** IOS with both policies

Unbalanced Schedule

No trade off between parallelization strategies

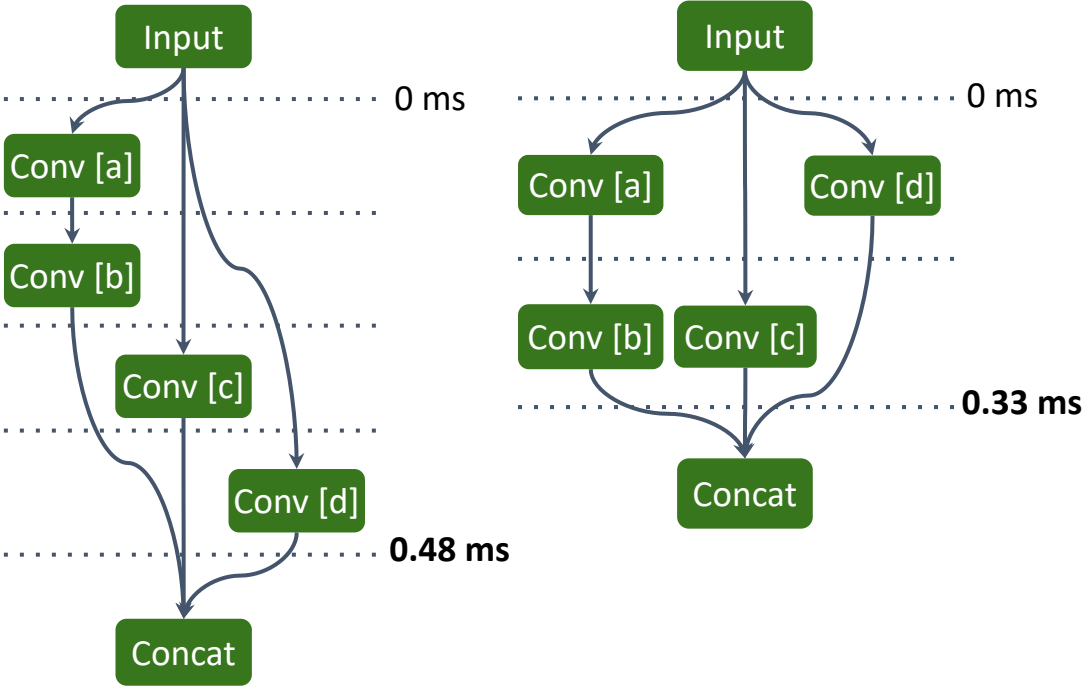
IOS Runtime



Performance is normalized to the best schedule

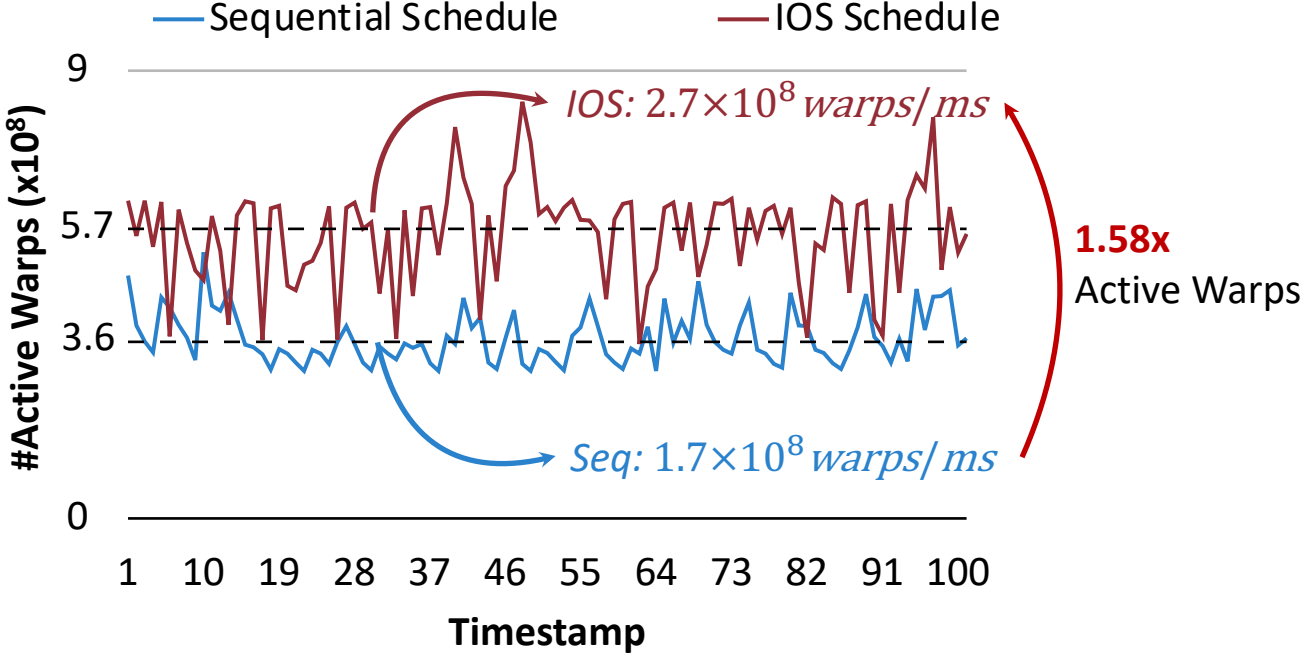
**IOS-Both** achieves the best performance

# More Active Warps Improve Utilization



Sequential Schedule

IOS Schedule



NVIDIA CUPTI profile frequency is every 2.1 ms.

More active warps → More eligible warps to execute at each cycle → Higher Device-Utilization

# Conclusion

- Sequential execution suffers from **under utilization** problem.
- Inter-Operator Scheduler (**IOS**):
  - Utilize both intra- and **inter-operator parallelism** in CNNs.
  - **Dynamic-programming** explores the schedule space **exhaustively**.
  - Time Complexity:  $\mathcal{O}\left((n/d + 1)^{2d}\right)$ ,  $d$  is usually small.
- Key Results: **1.1-1.5x** speedup on diverse CNNs.



<https://github.com/mit-han-lab/inter-operator-scheduler>

We provide scripts to reproduce results in every figure and table!

