Cortex: A Compiler For Recursive Deep Learning Models

Pratik Fegade[1],
Tianqi Chen[1,2], Phillip B. Gibbons[1], Todd C. Mowry[1]

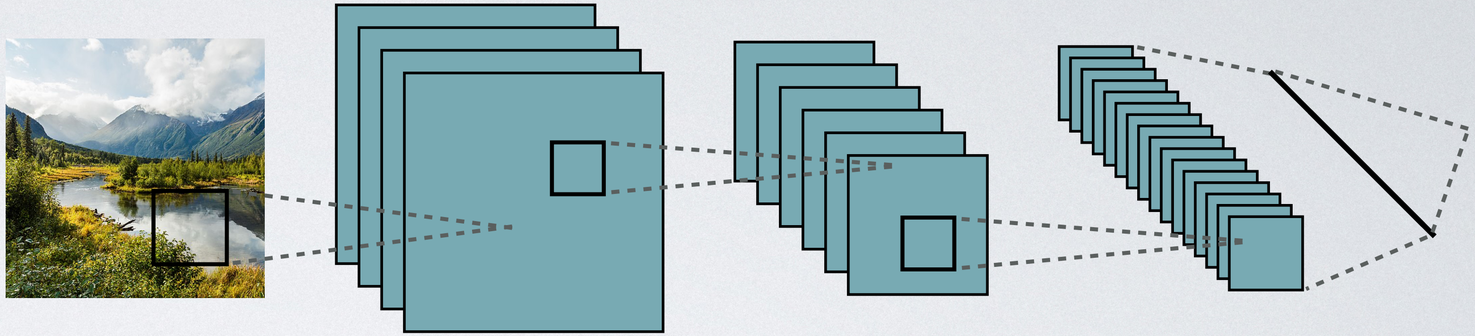
[1]Carnegie Mellon University [2]OctoML

Carnegie Mellon University
Computer Science Department

catalyst

Deep Learning Models Often Mirror Input Structure

- Convolutional neural networks



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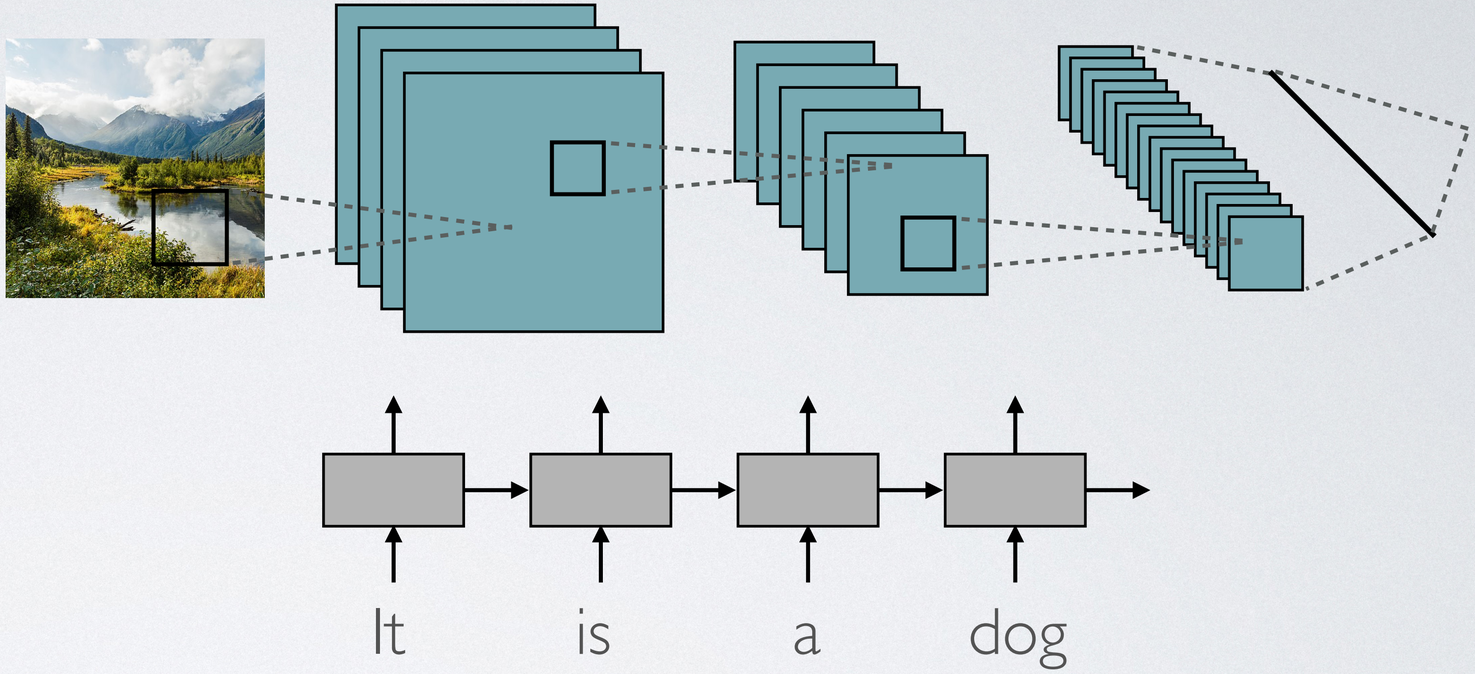

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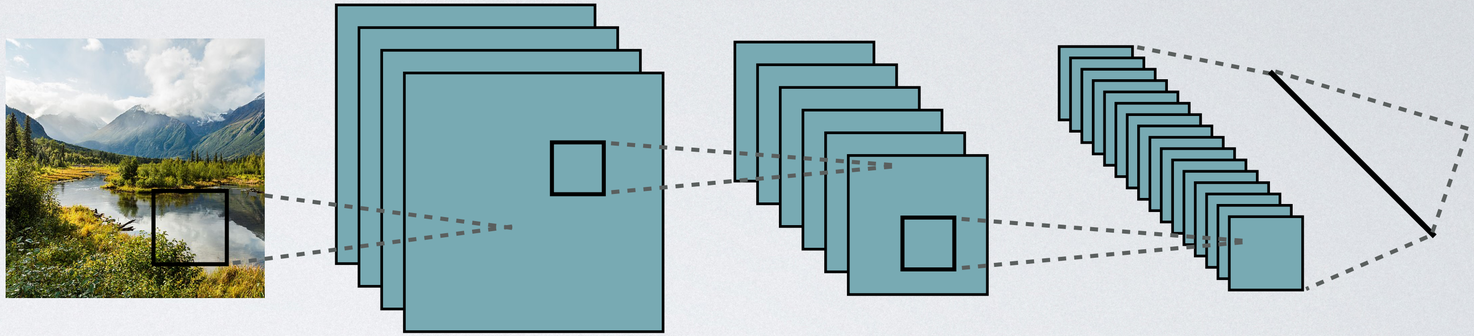
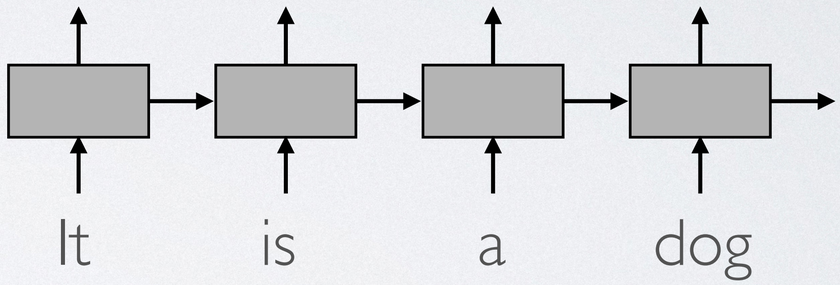
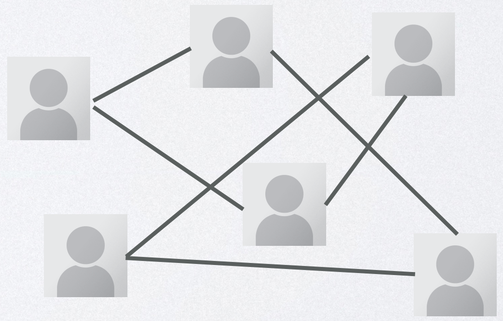
- Graph neural networks







Recursive Input Domains Lead to Recursive Models

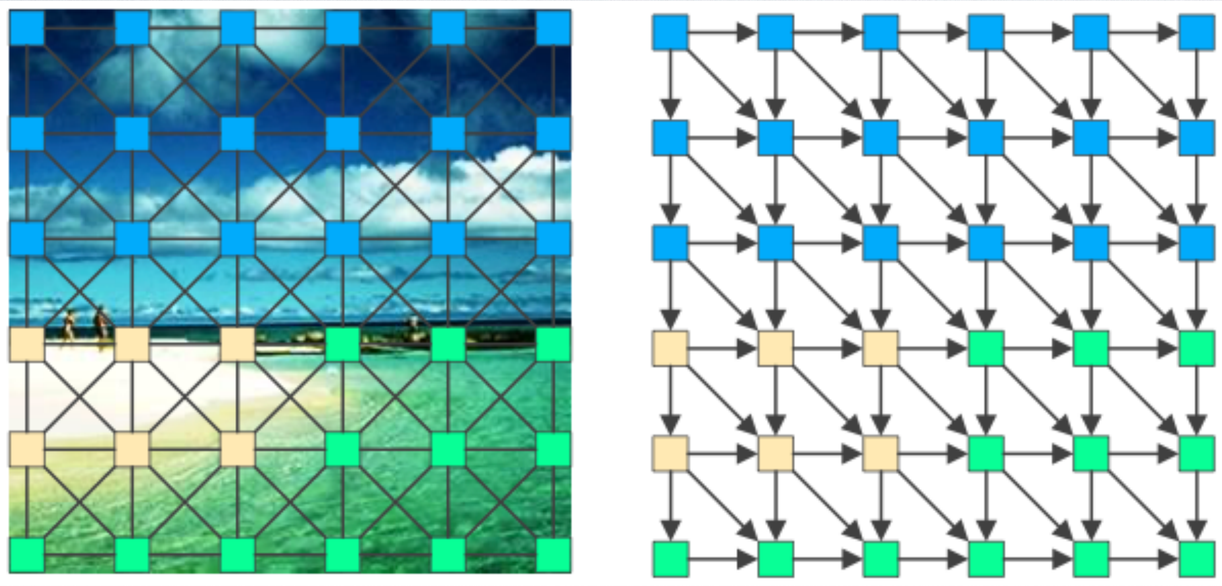


Image segmentation using DAG-RNN

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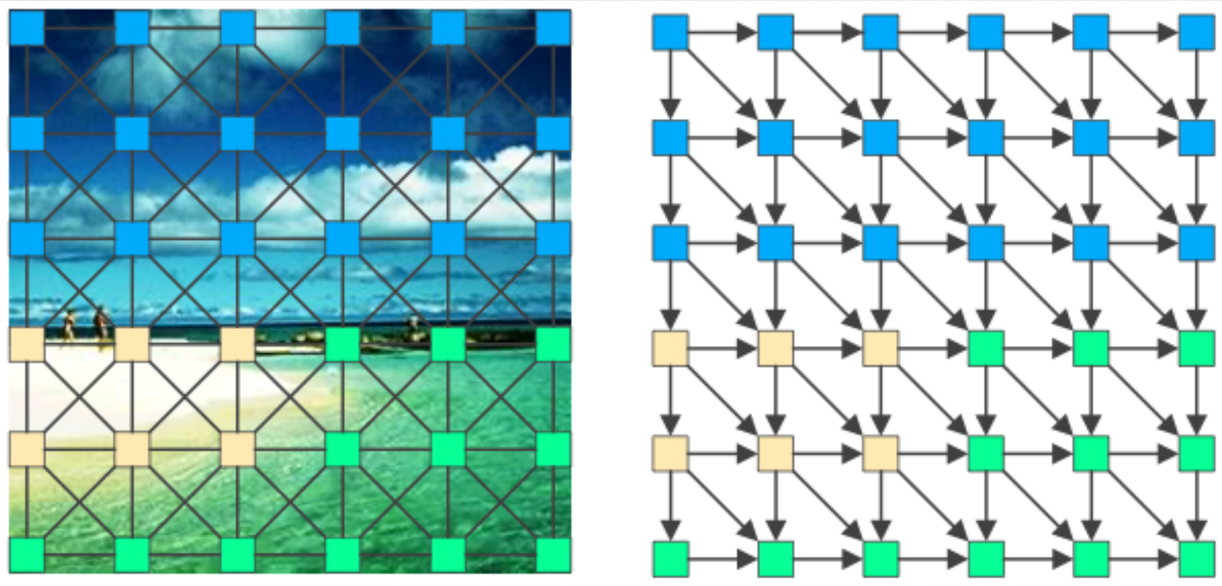

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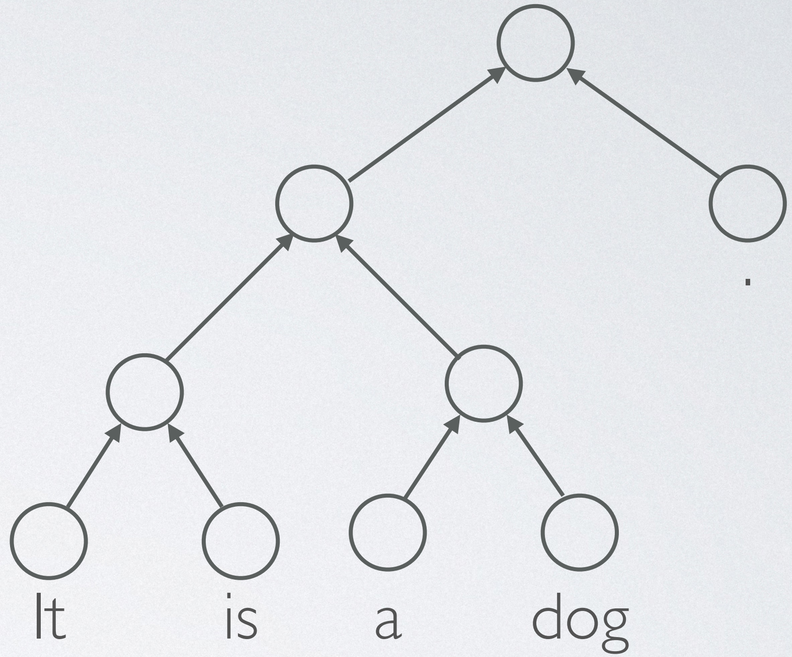

Semantic text classification using TreeLSTM

Outline

- Motivation: Inefficiencies in Execution of Recursive Models
- Cortex: Our Compiler Based Solution
  - Recursive Lowering
  - Loop IR Lowering
- Evaluation
- Conclusion

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Running Example: Simple TreeFC Model

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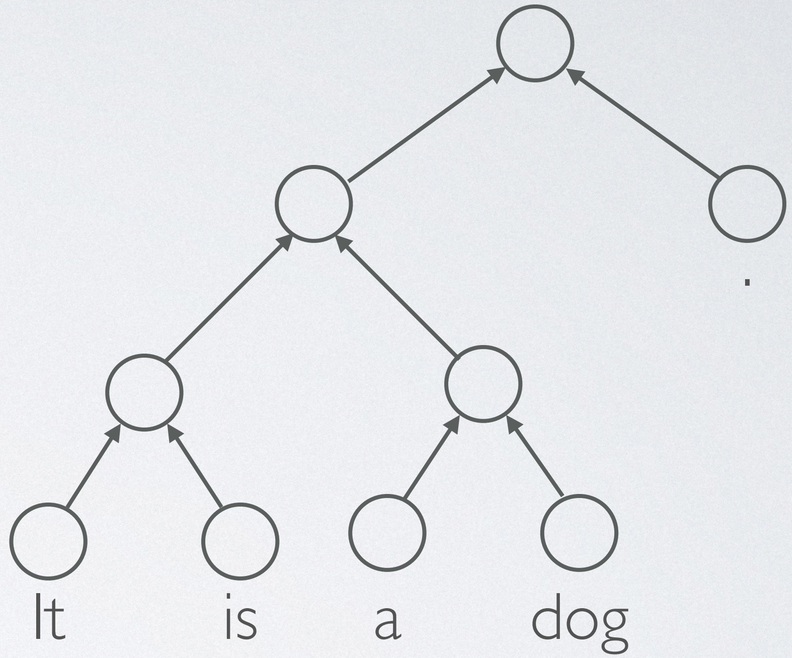

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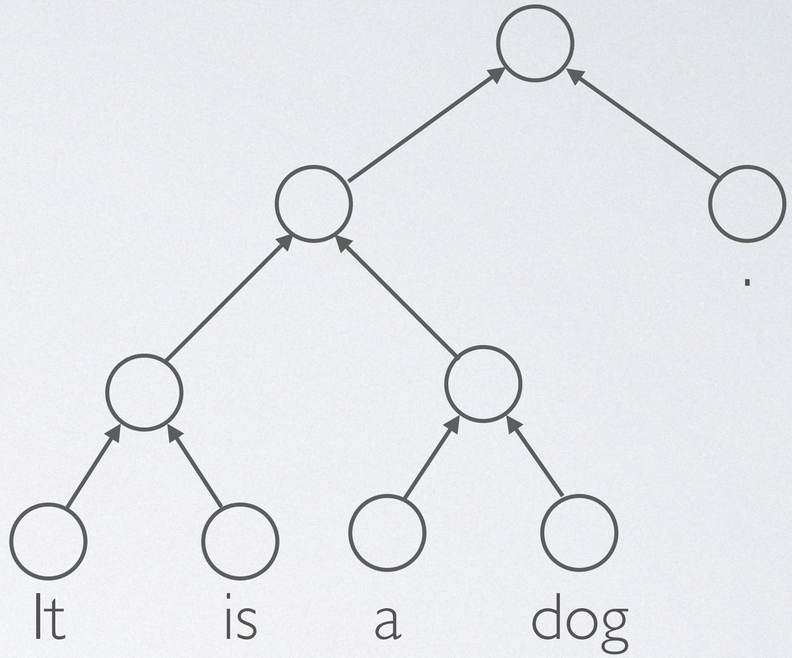

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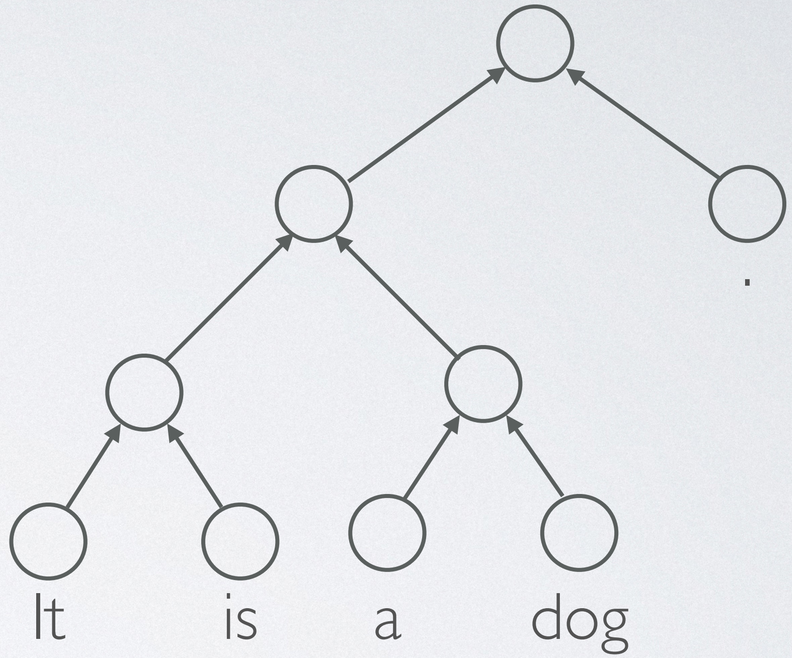

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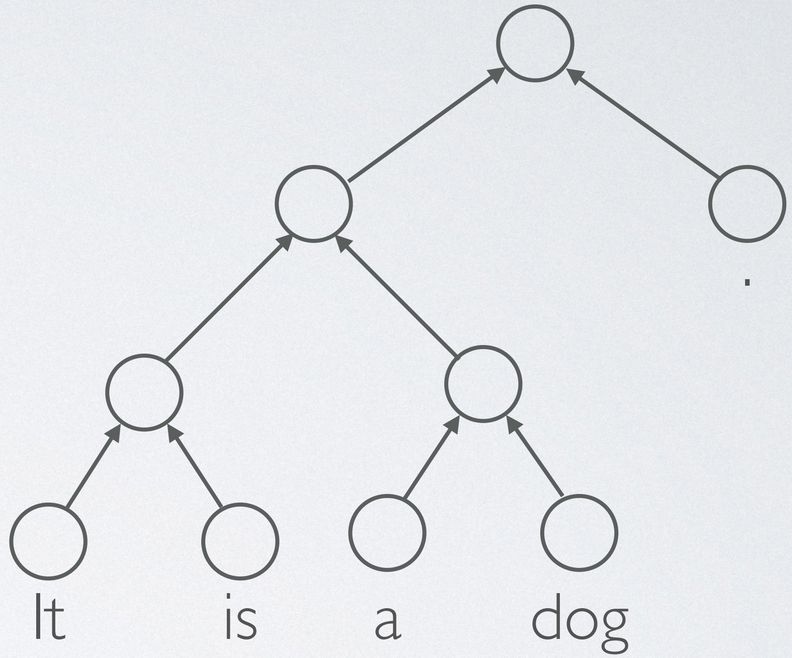

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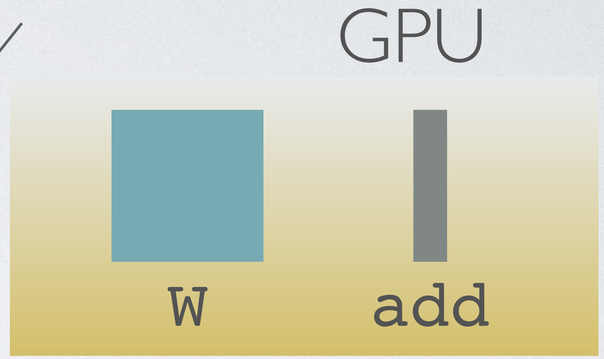

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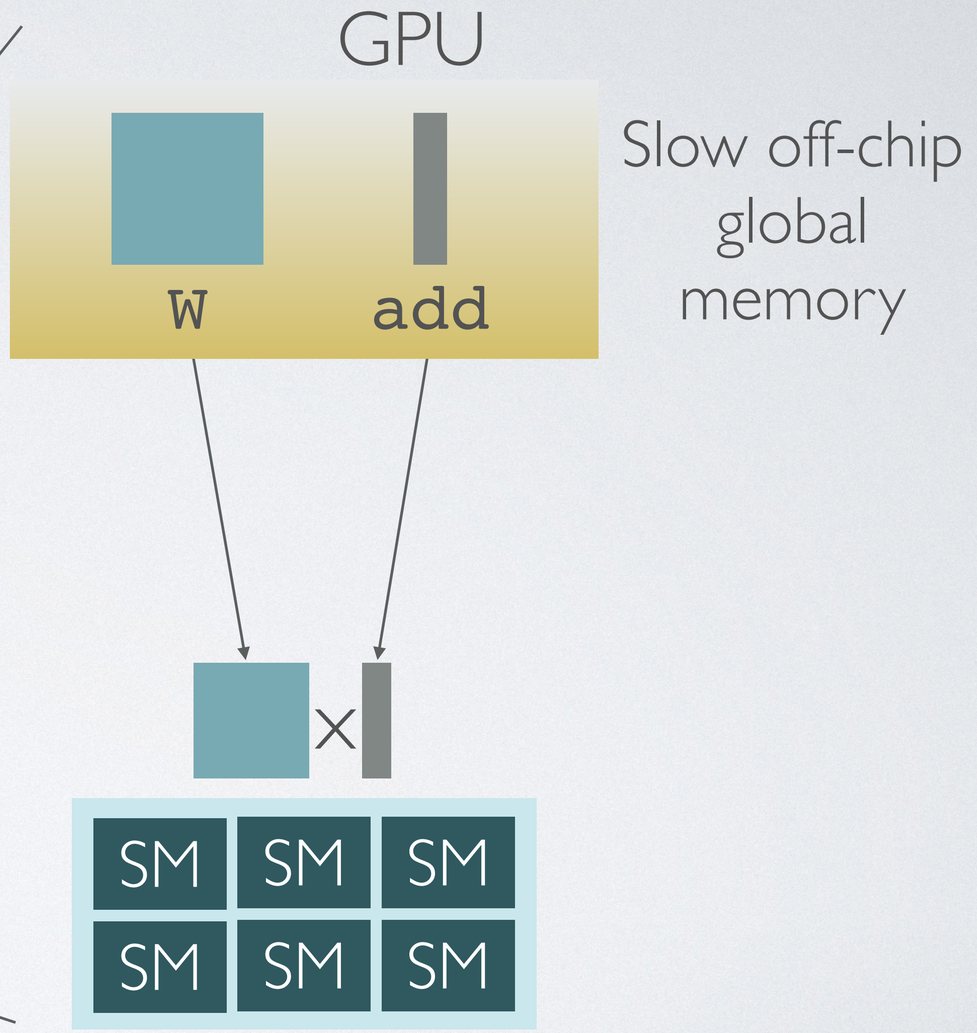

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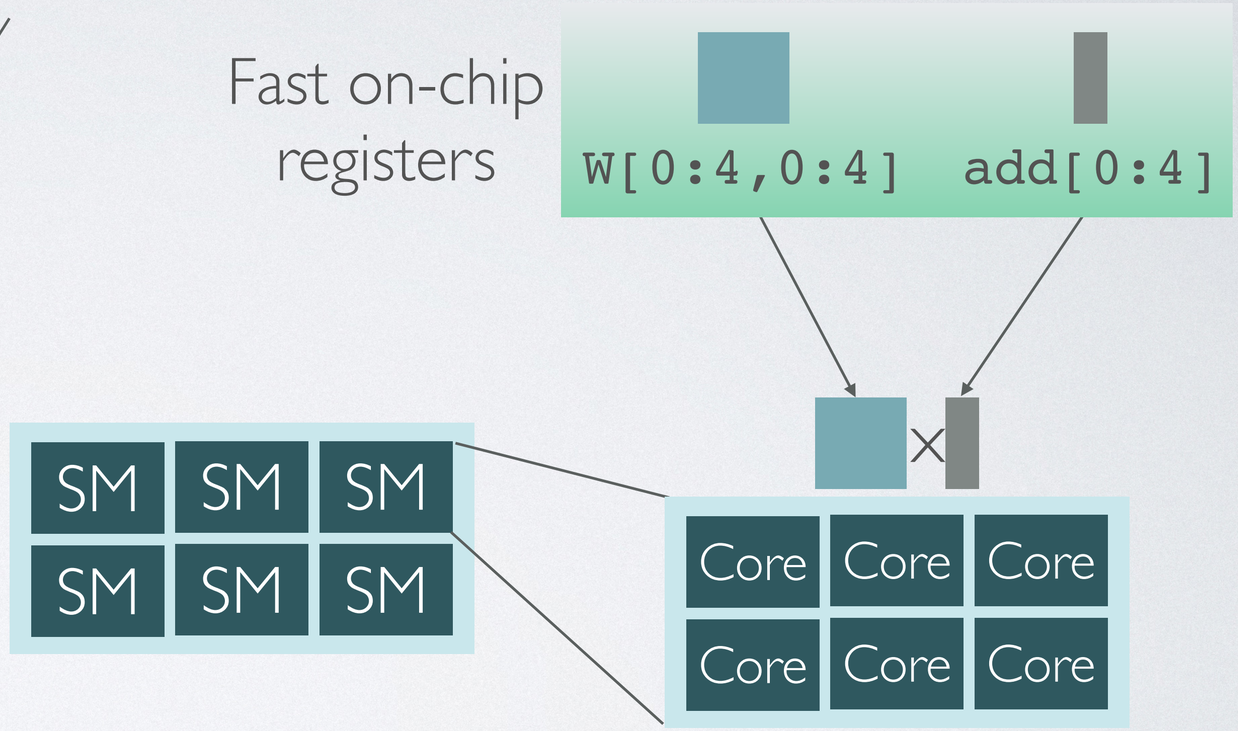

Challenges With Aggressive Kernel Fusion

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- Can no longer use vendor libraries

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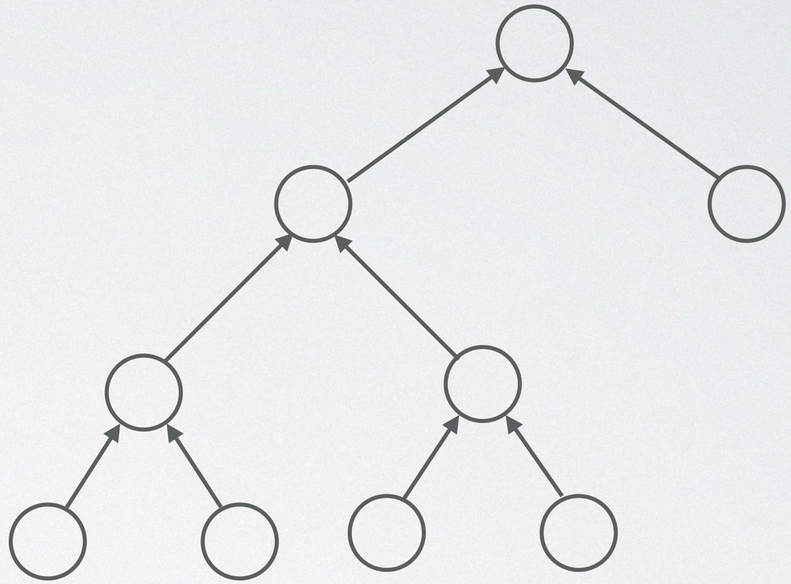

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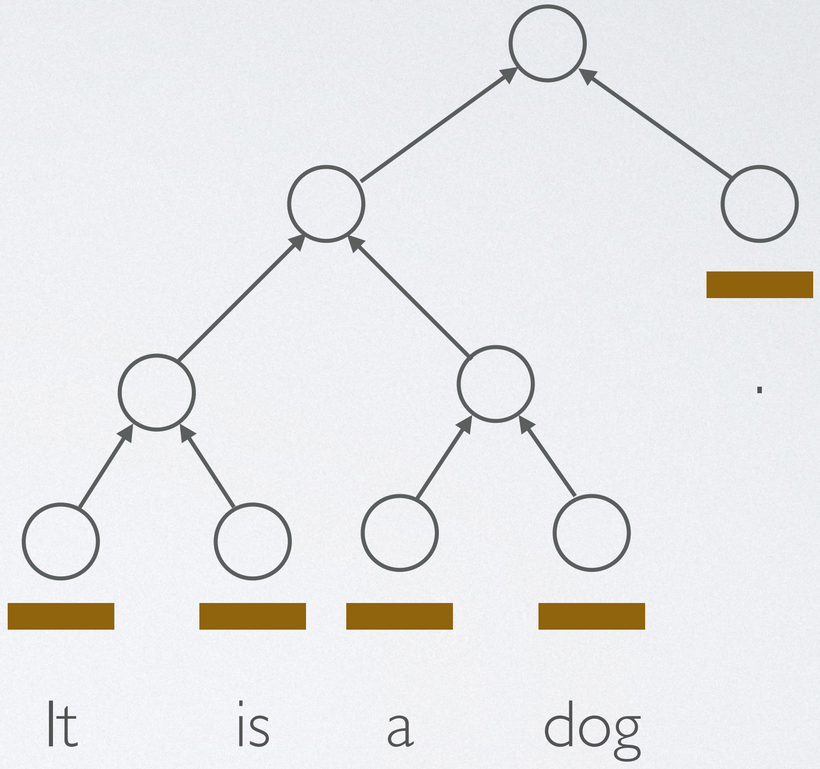

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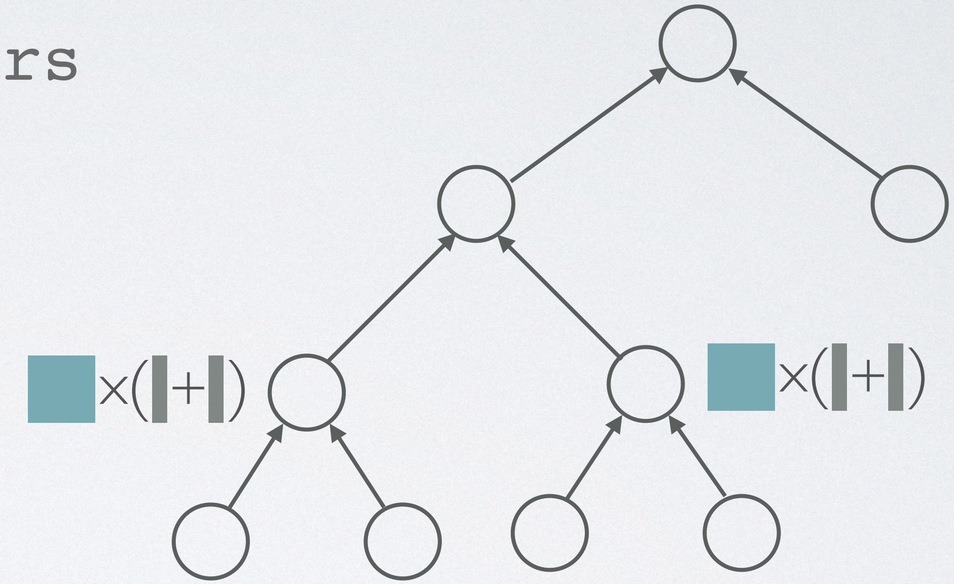

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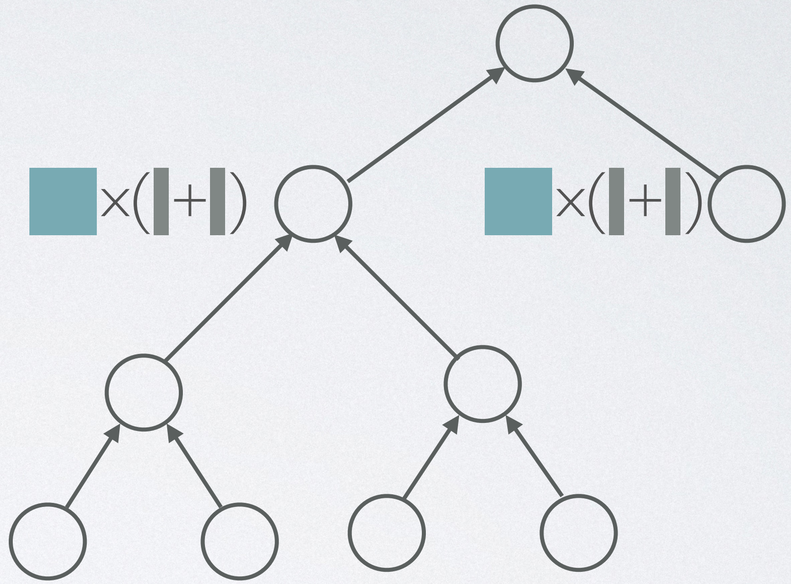

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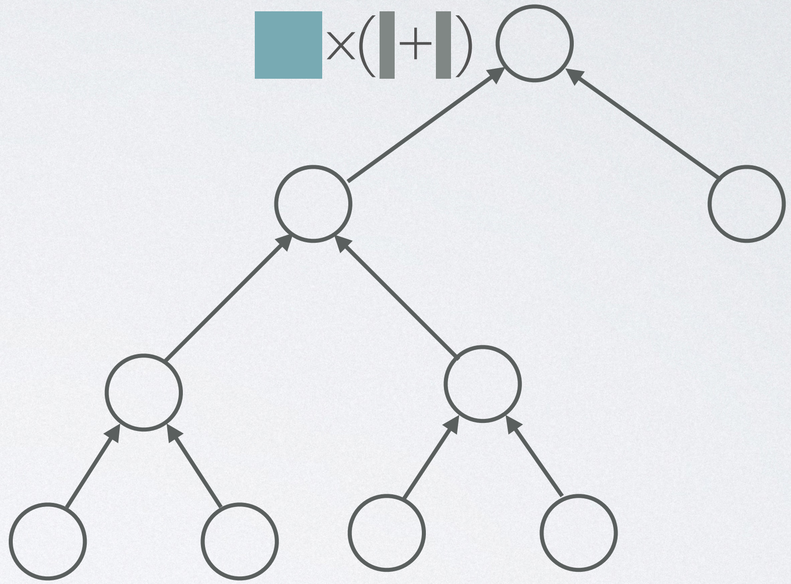

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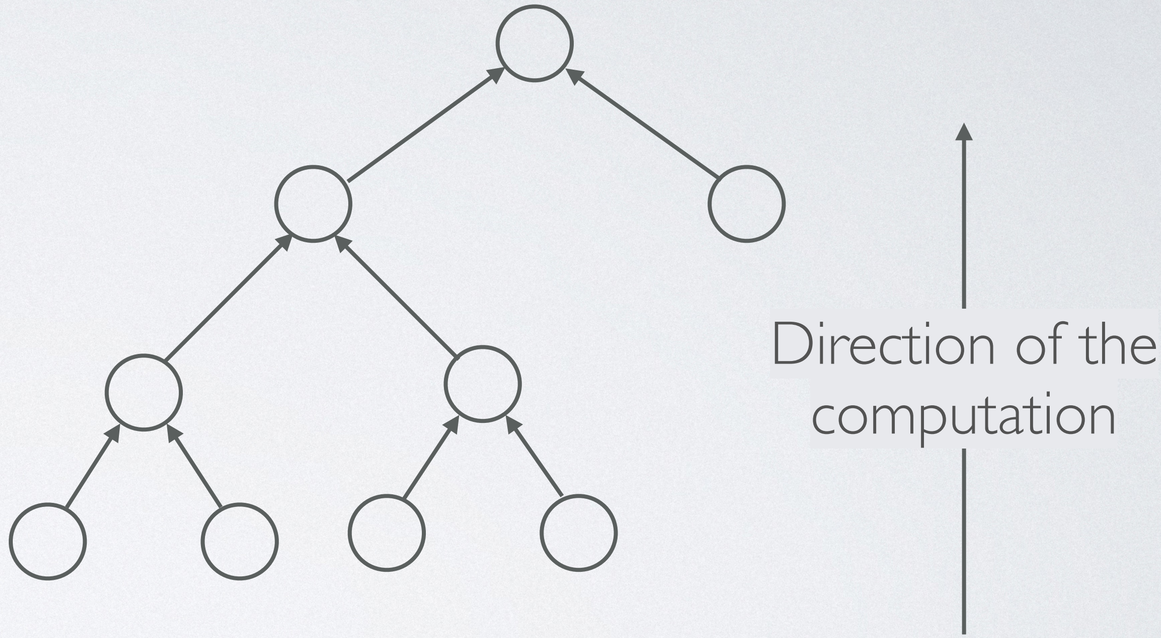

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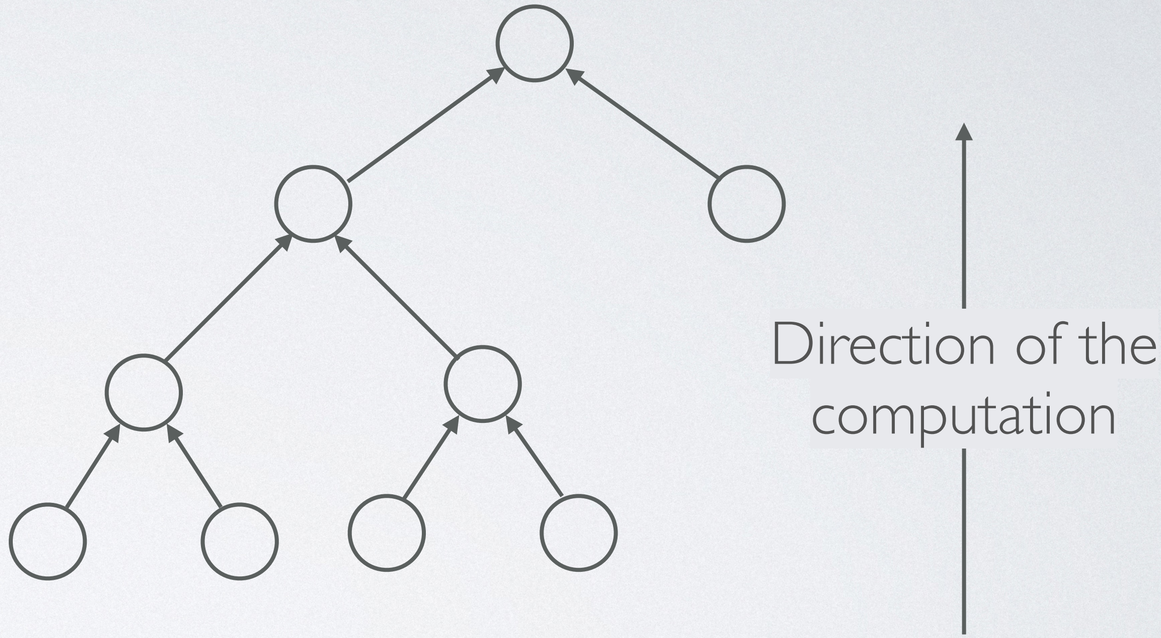

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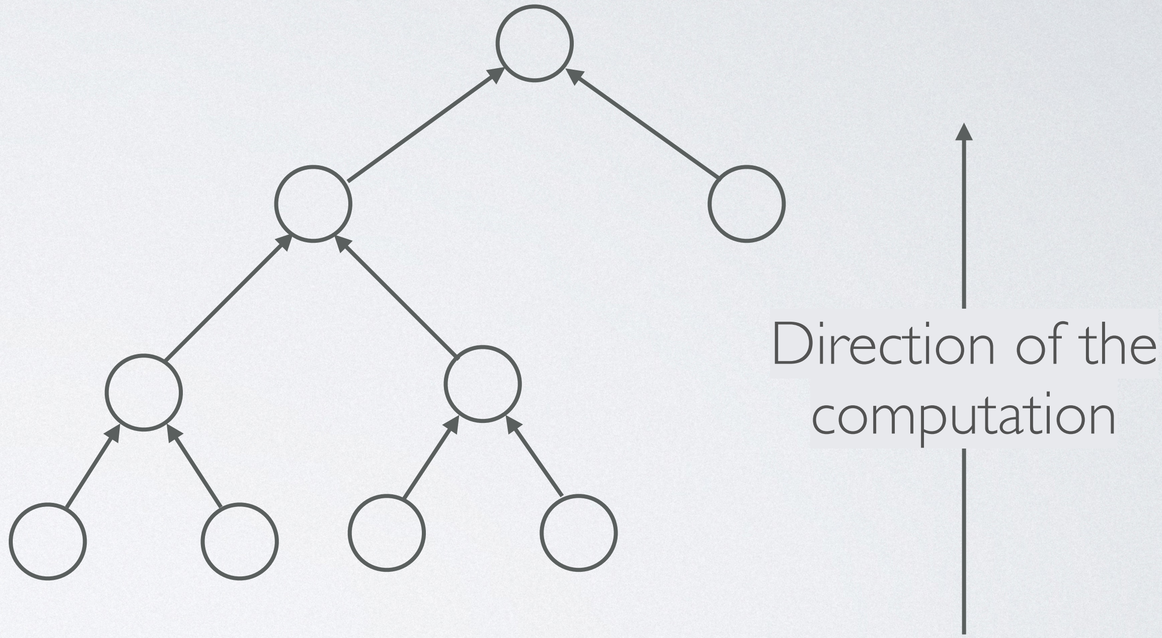

Data Structure Linearization in Cortex

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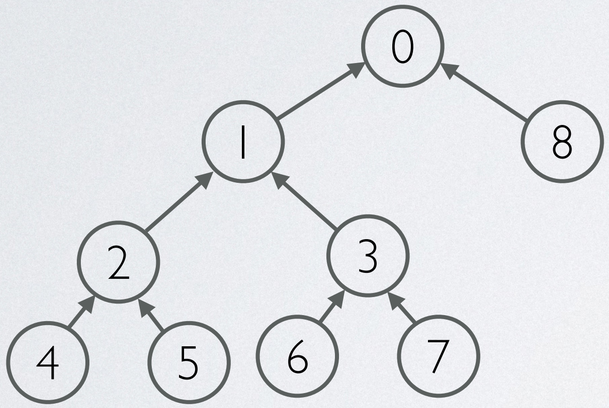

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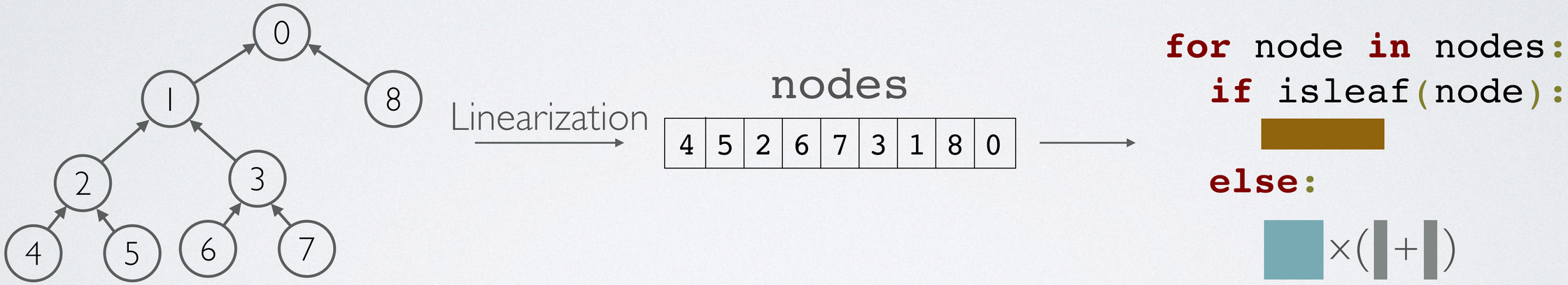
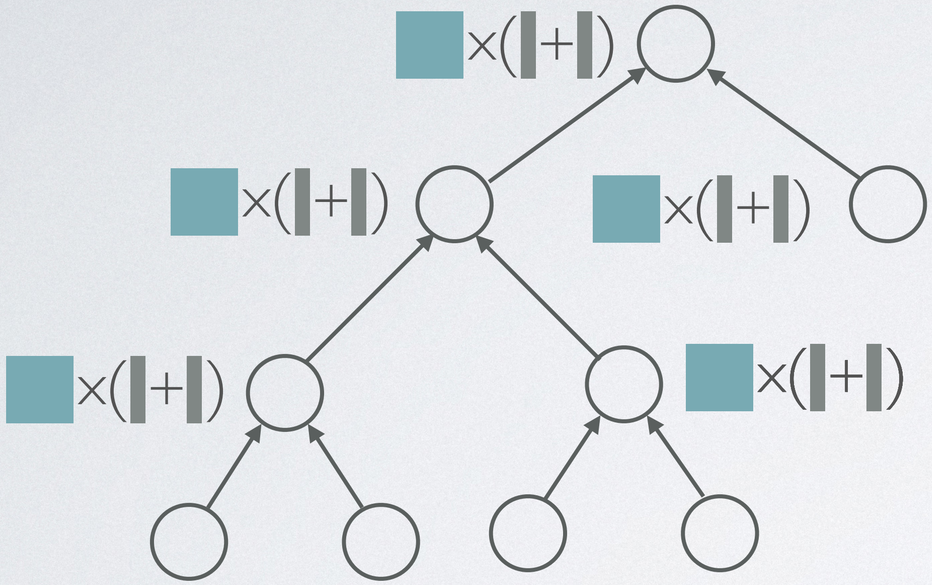


Separation of Control Flow and Tensor Computations



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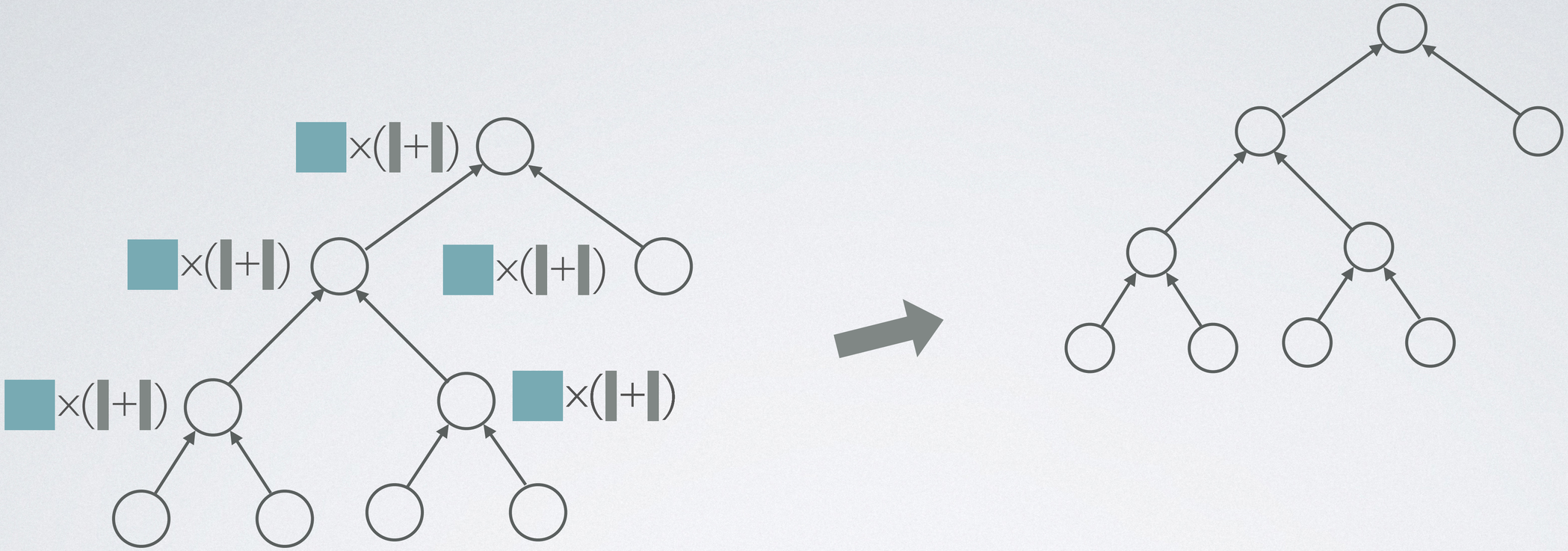

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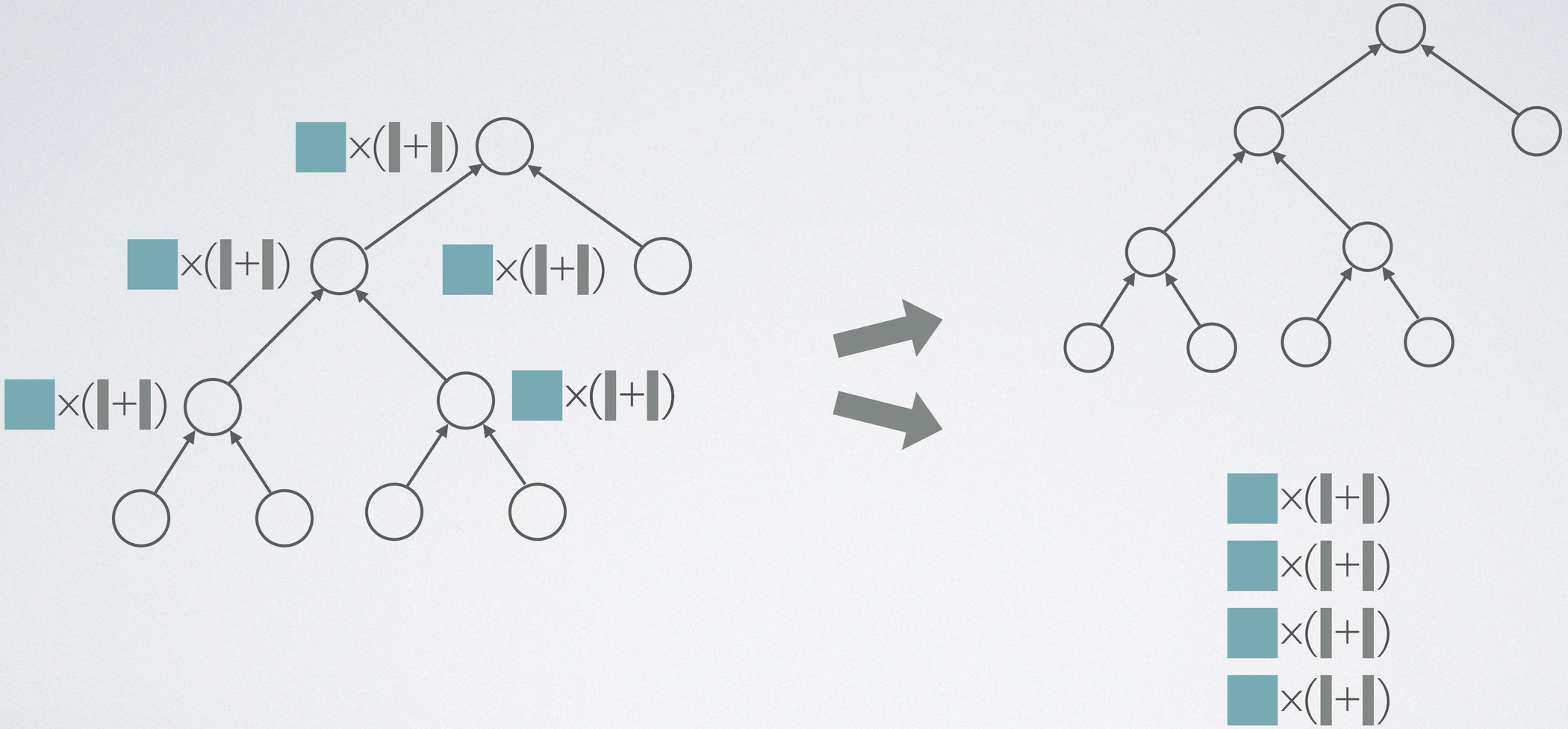

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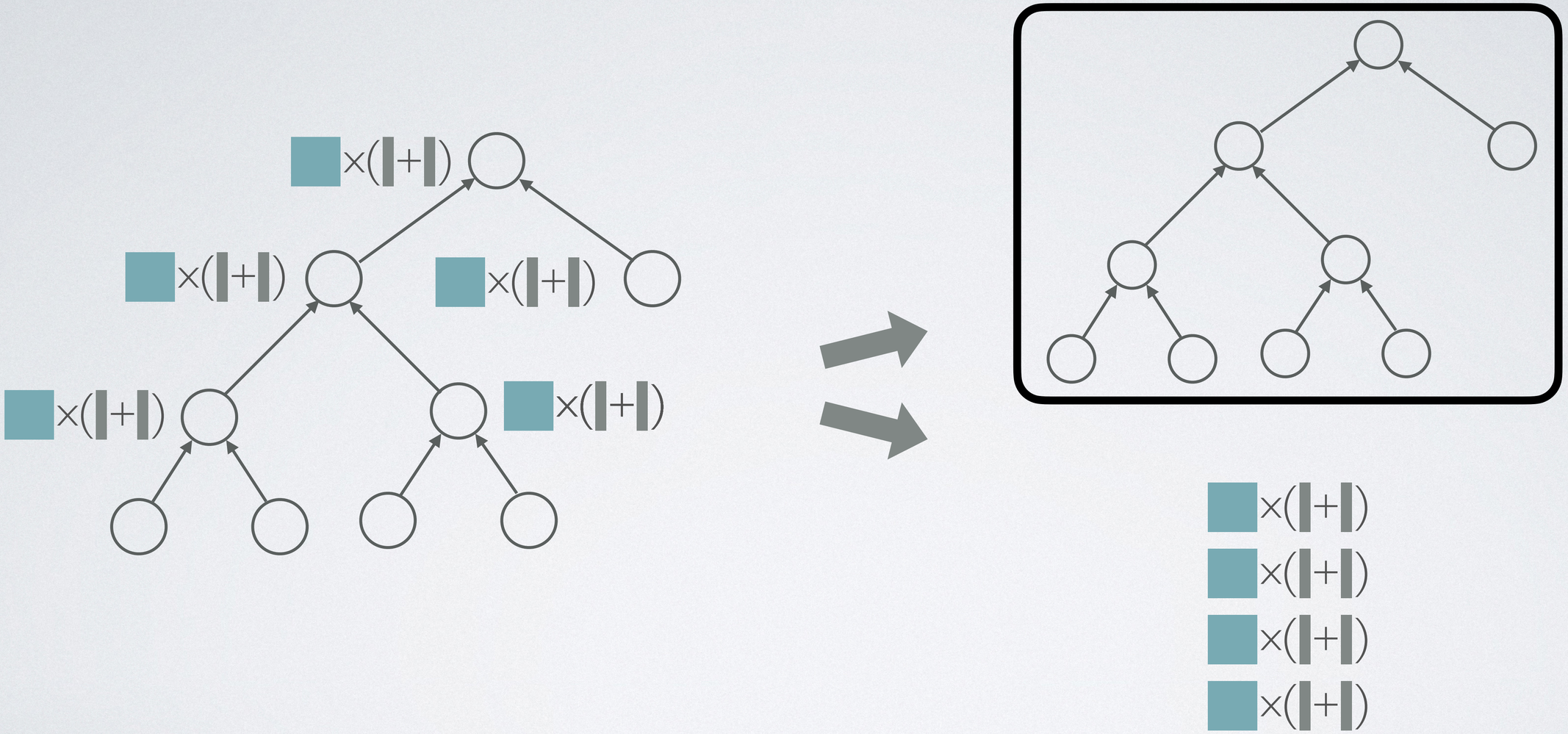

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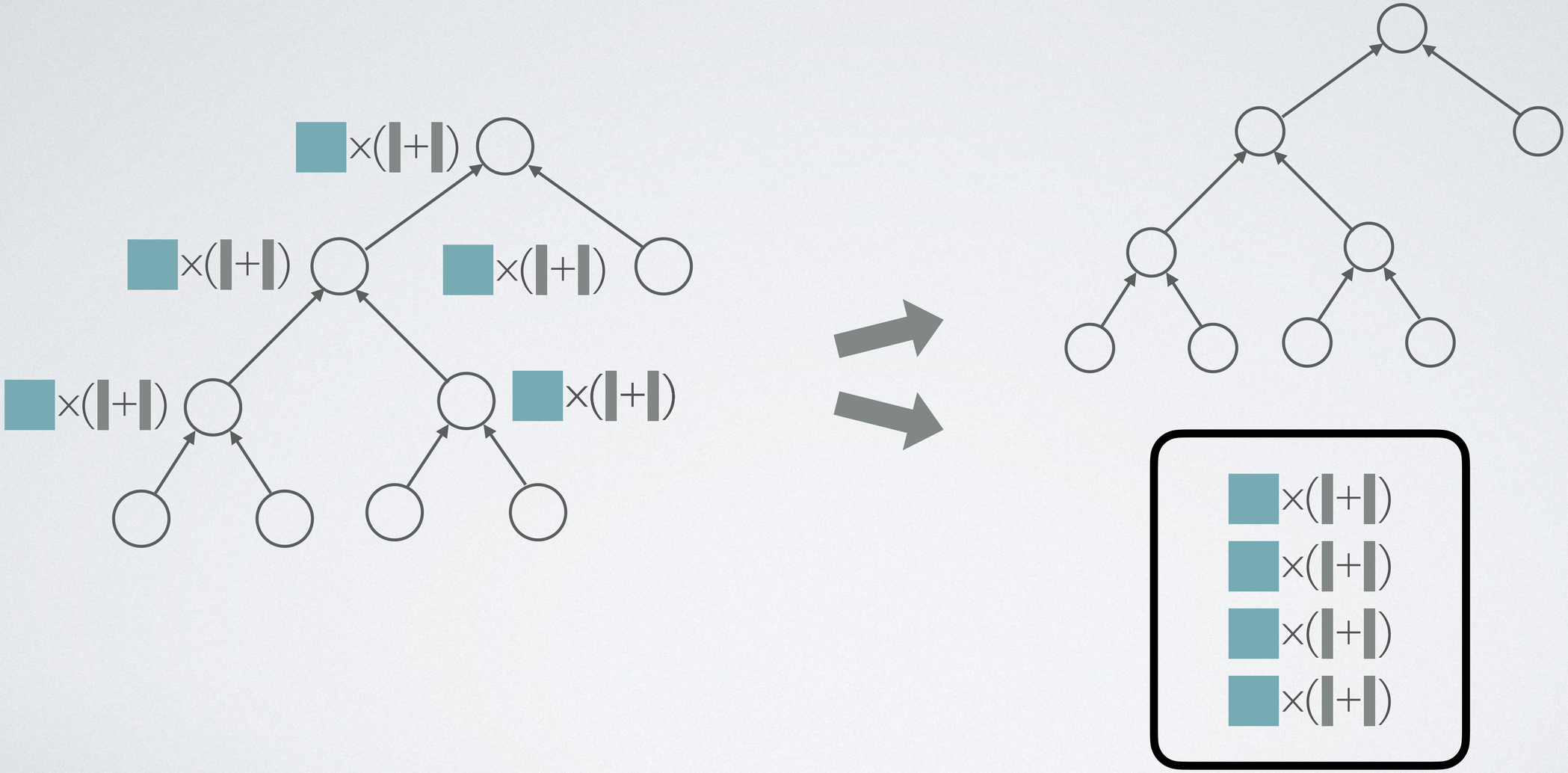

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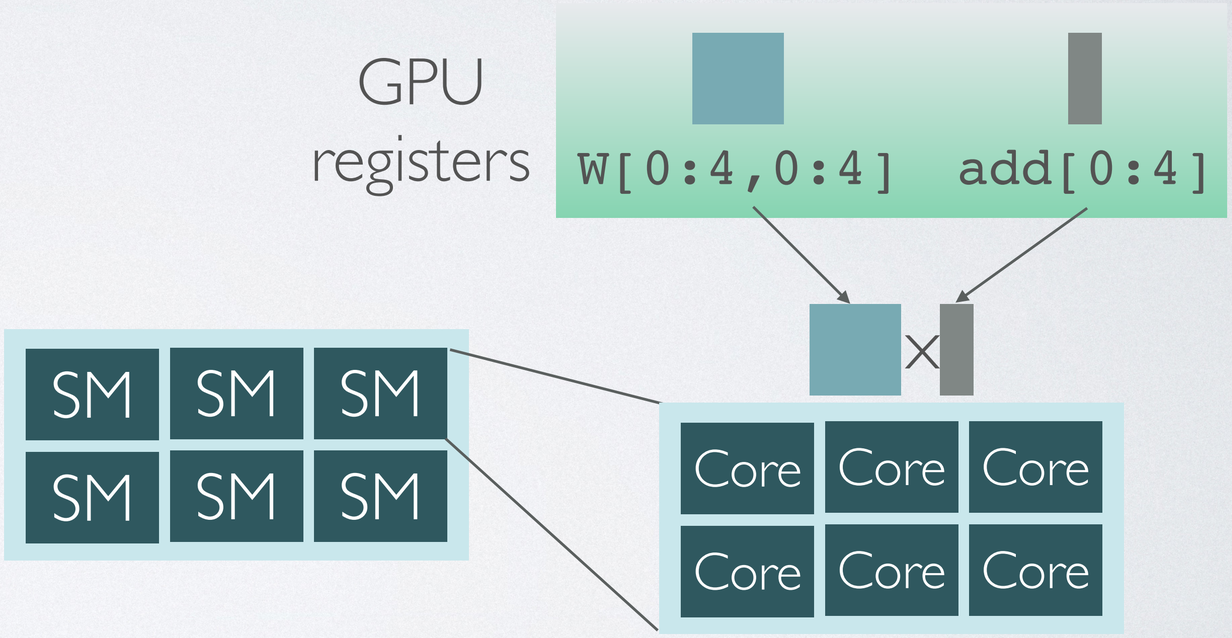

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Input recursive model computation

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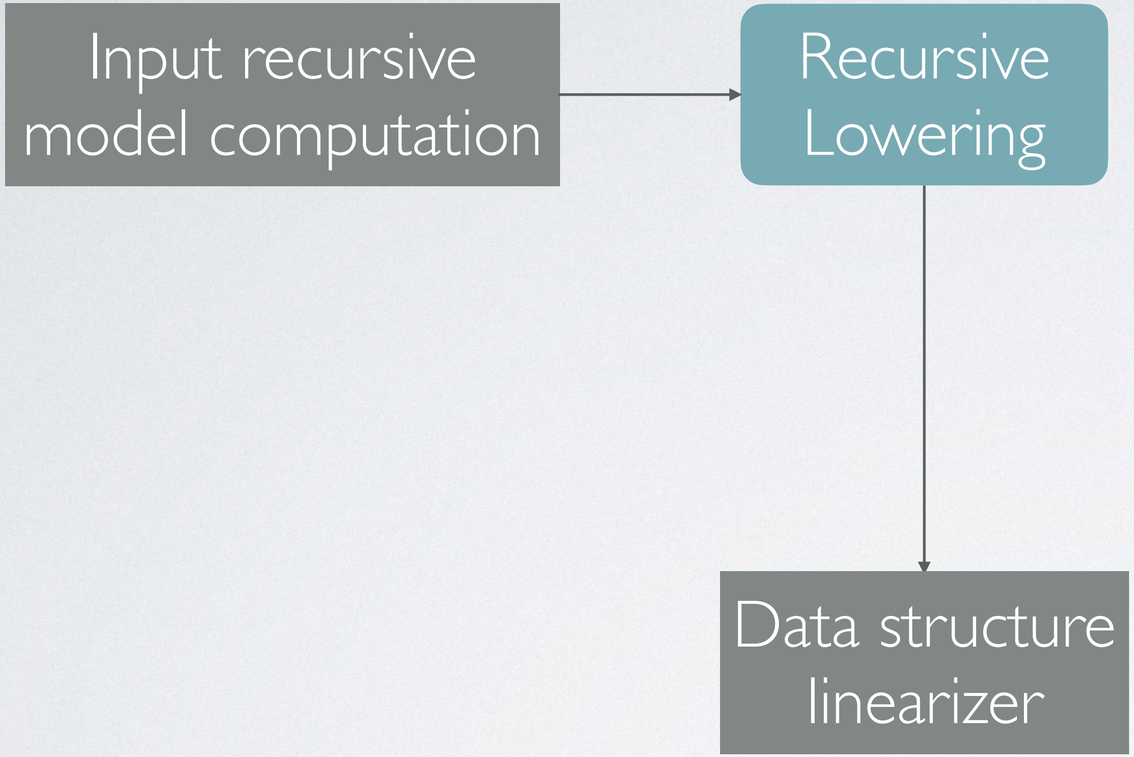

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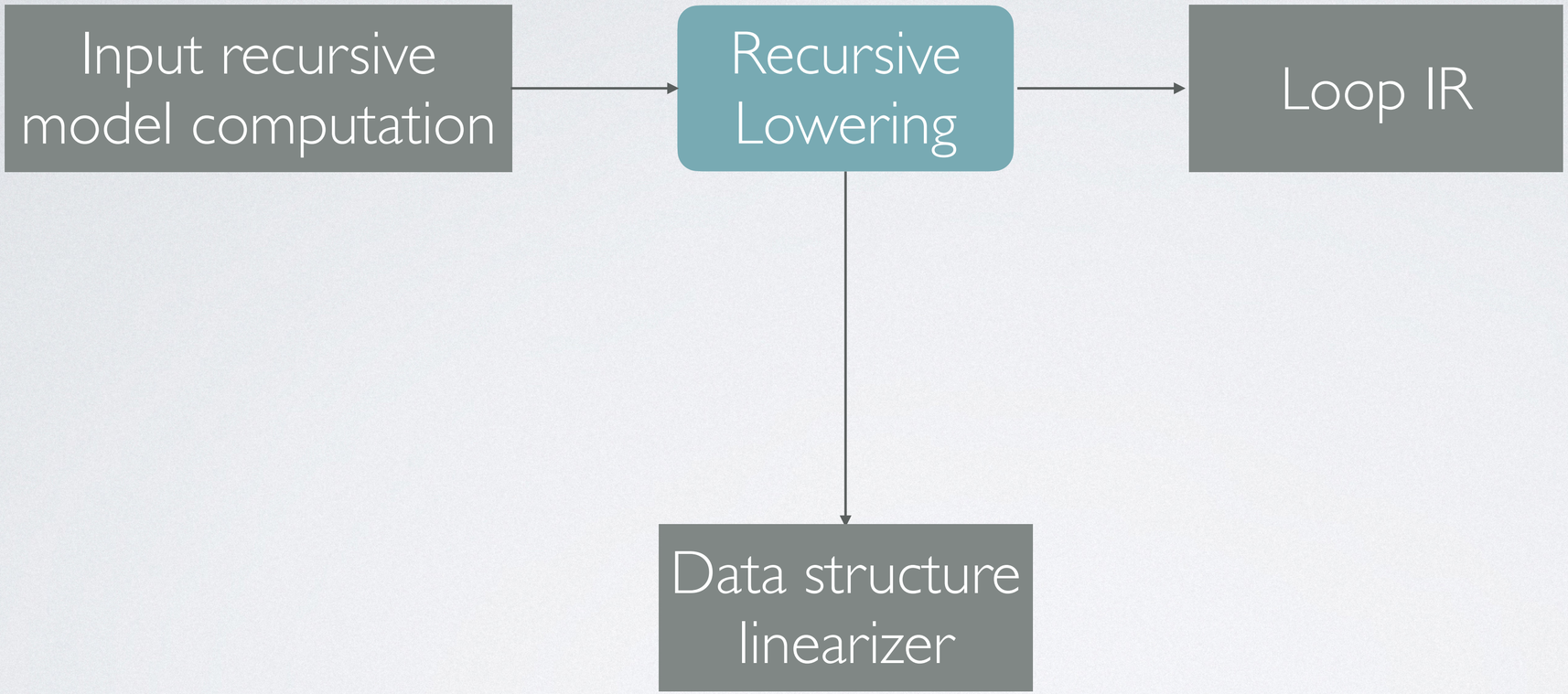

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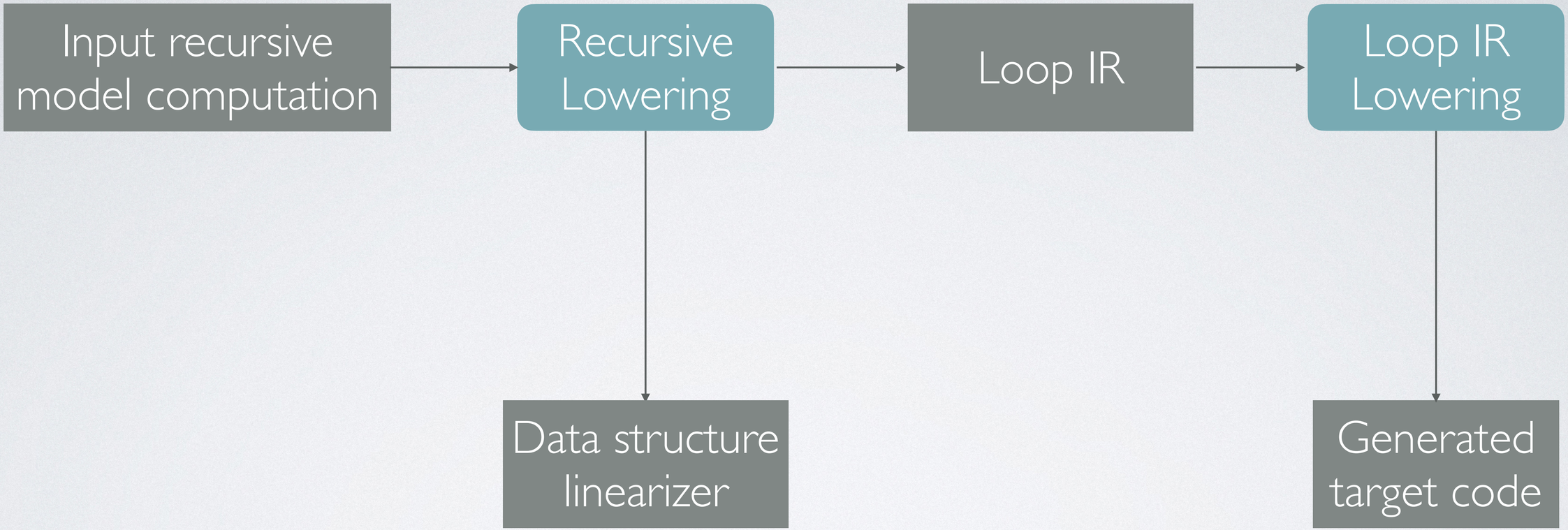

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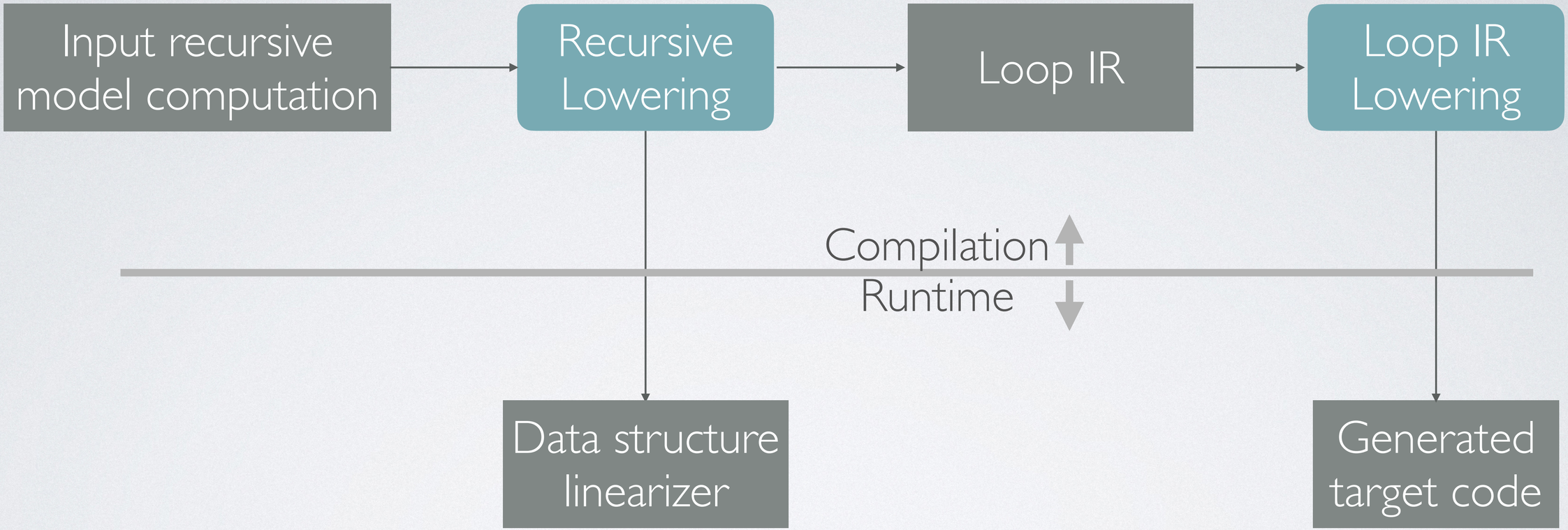

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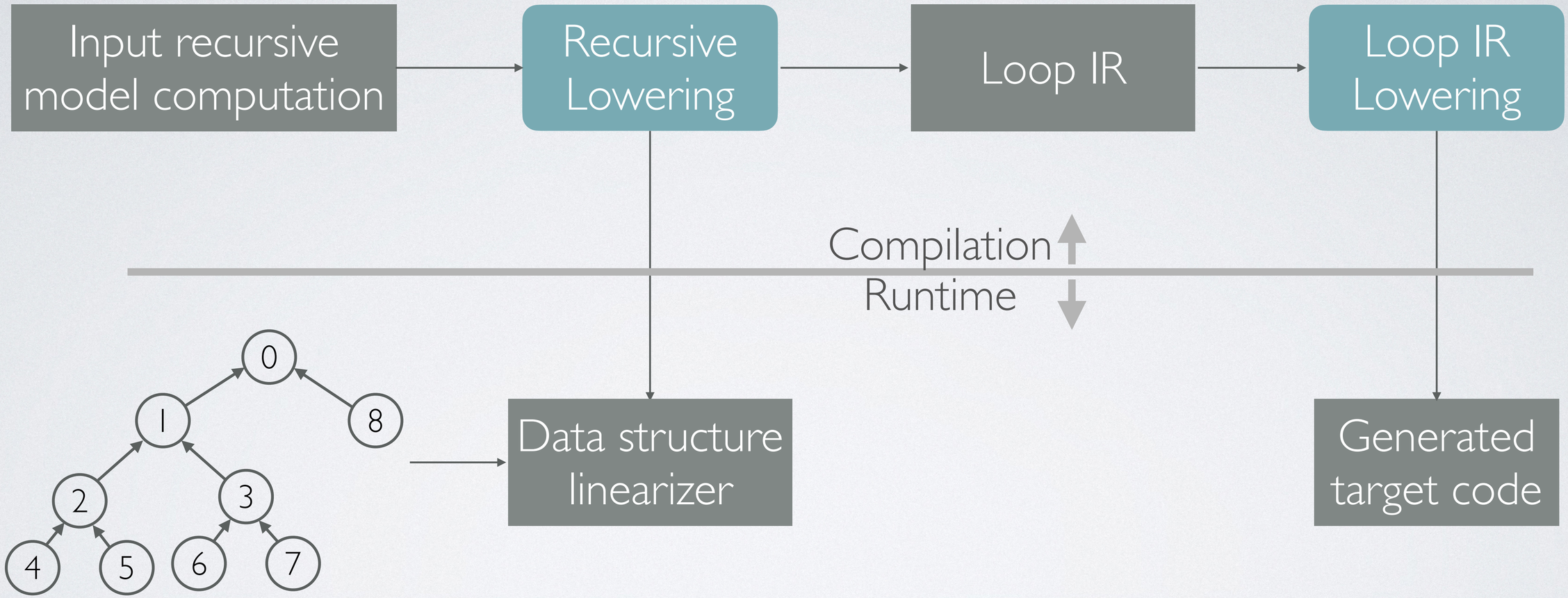

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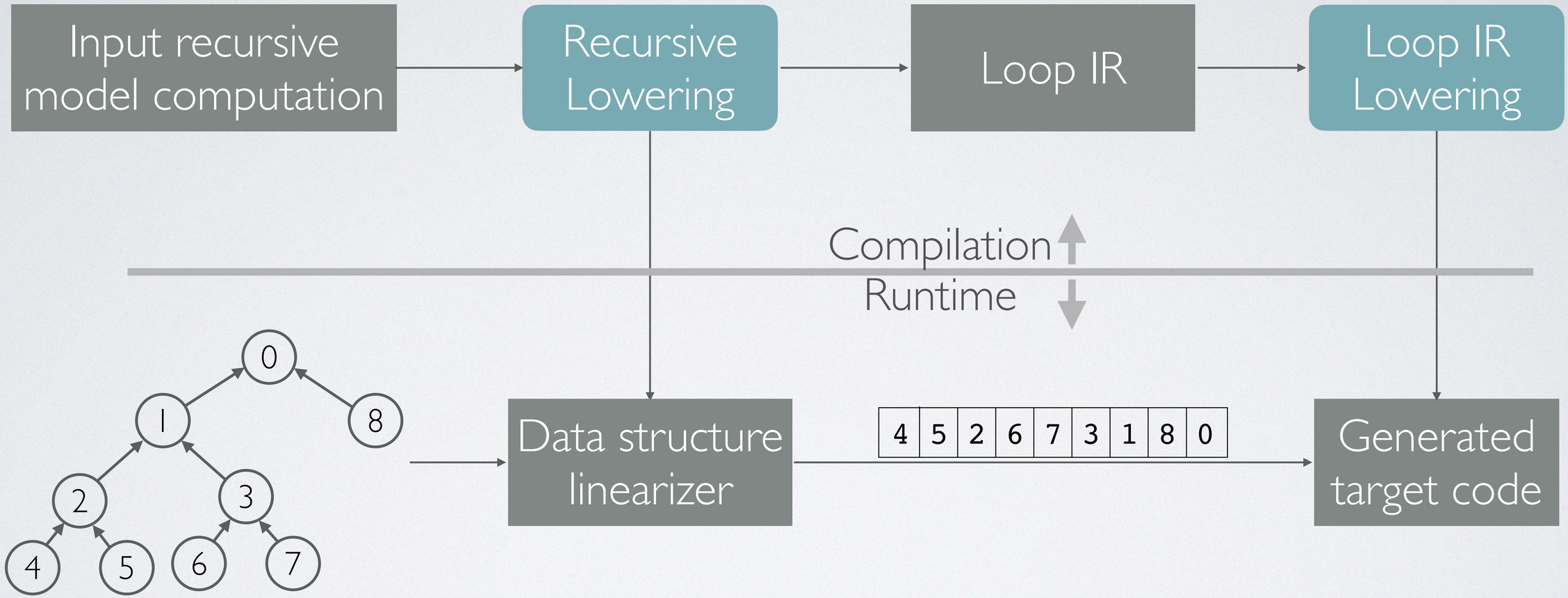

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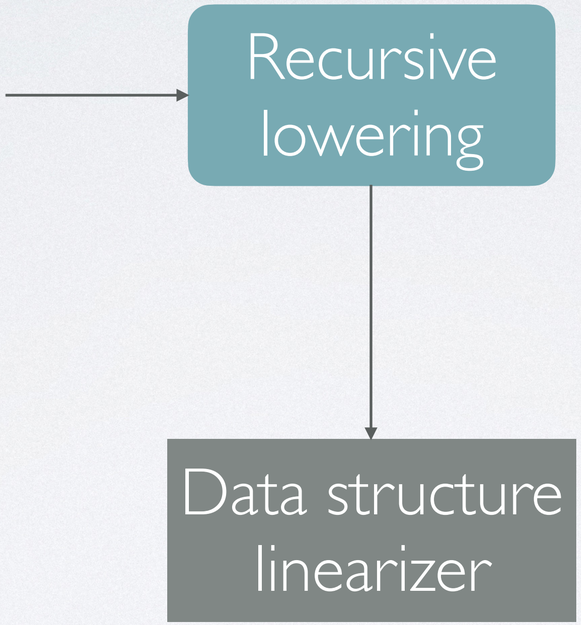

Recursion Is Lowered to Efficient Loops

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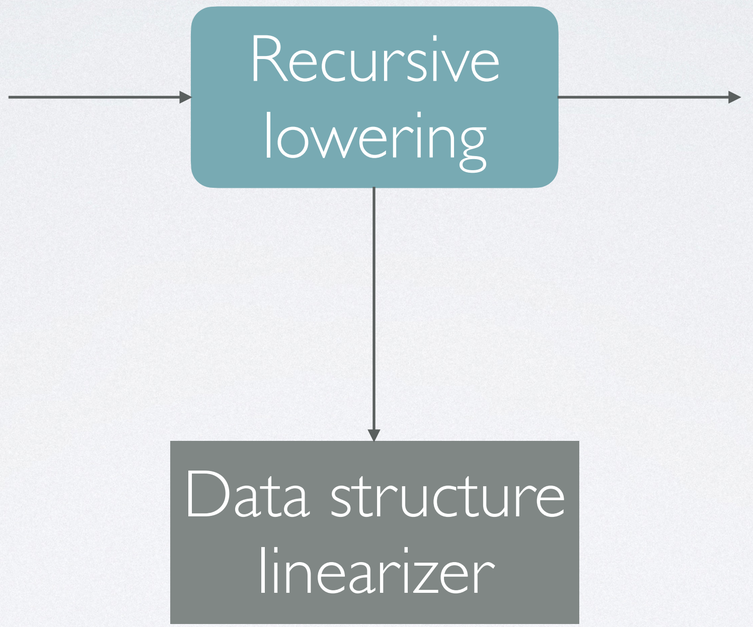


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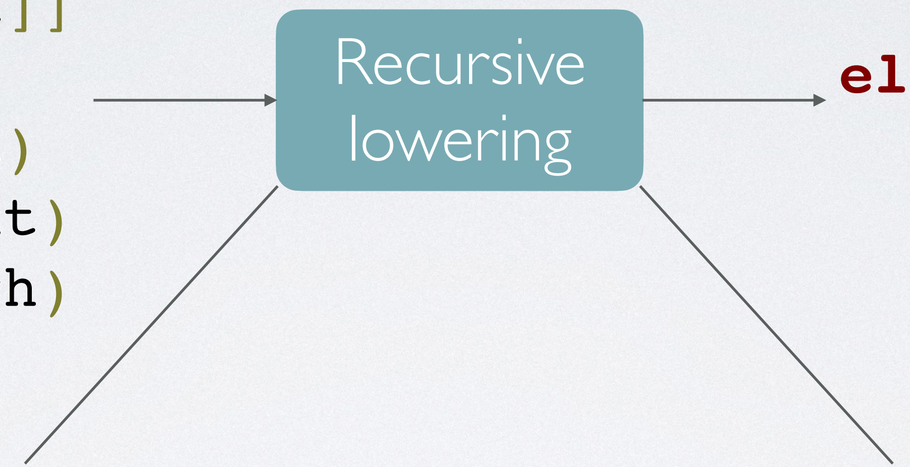


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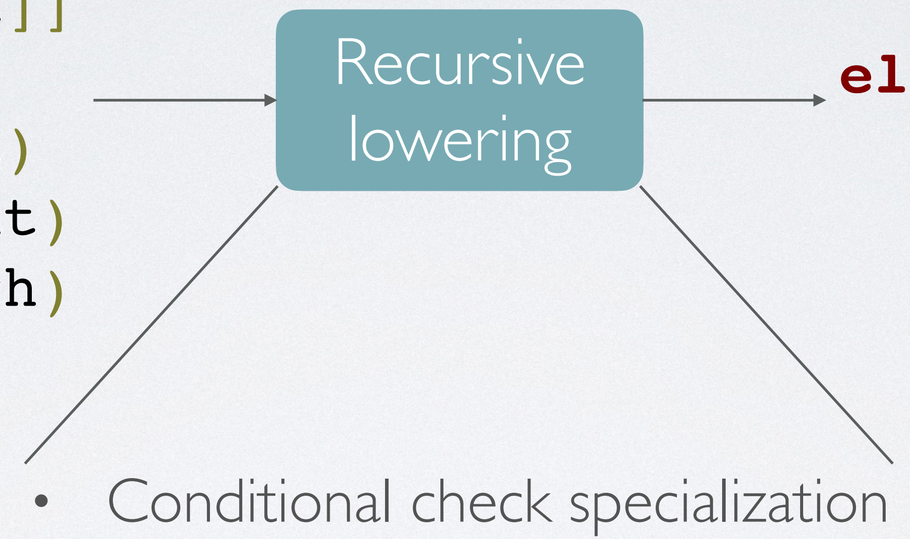


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- Conditional check specialization

Recursion Is Lowered to Efficient Loops

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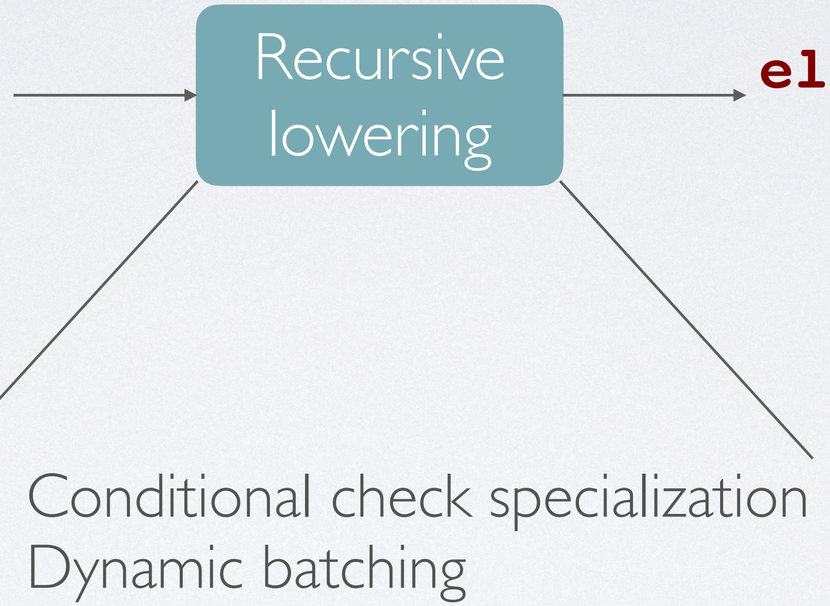


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- Conditional check specialization
- Dynamic batching

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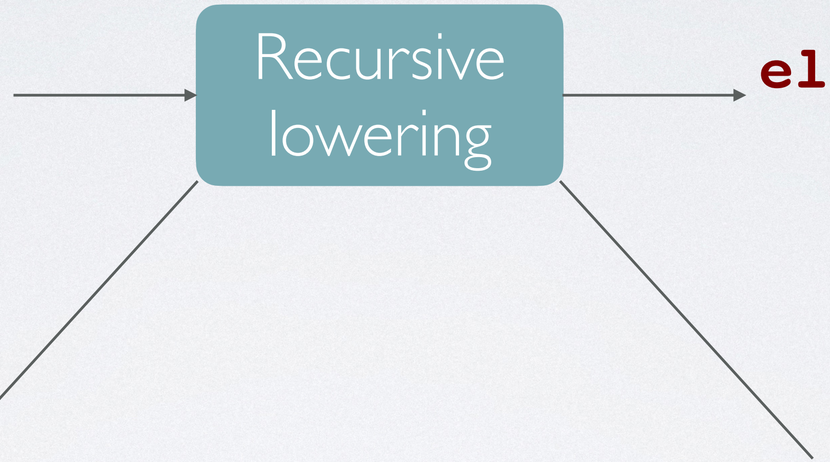


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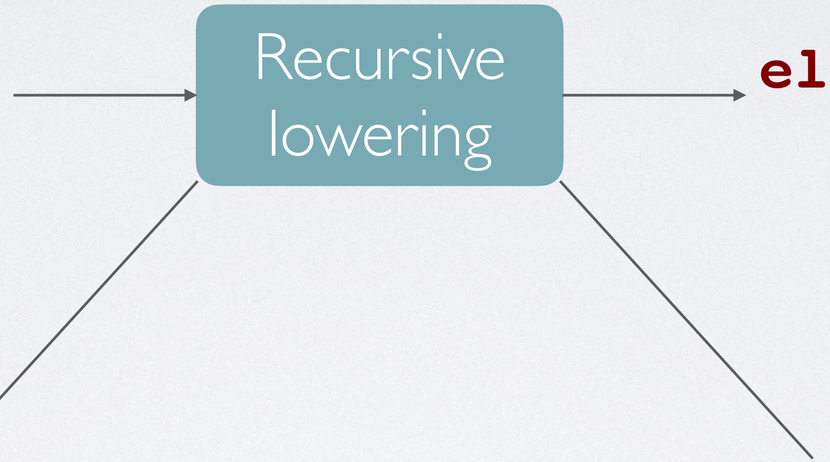


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- Conditional check specialization
- Dynamic batching
- Recursive unrolling
- Recursive refactoring

Cortex Provides Recursive Scheduling Primitives

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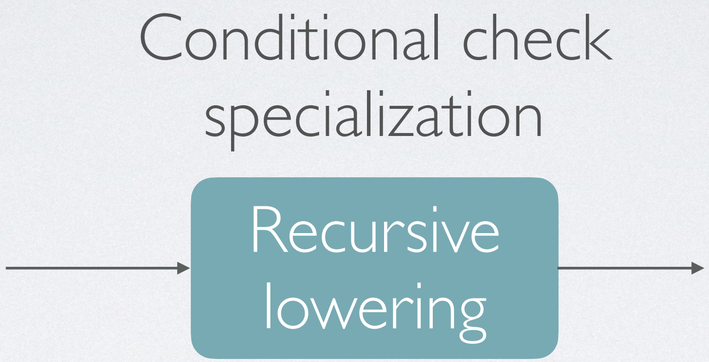


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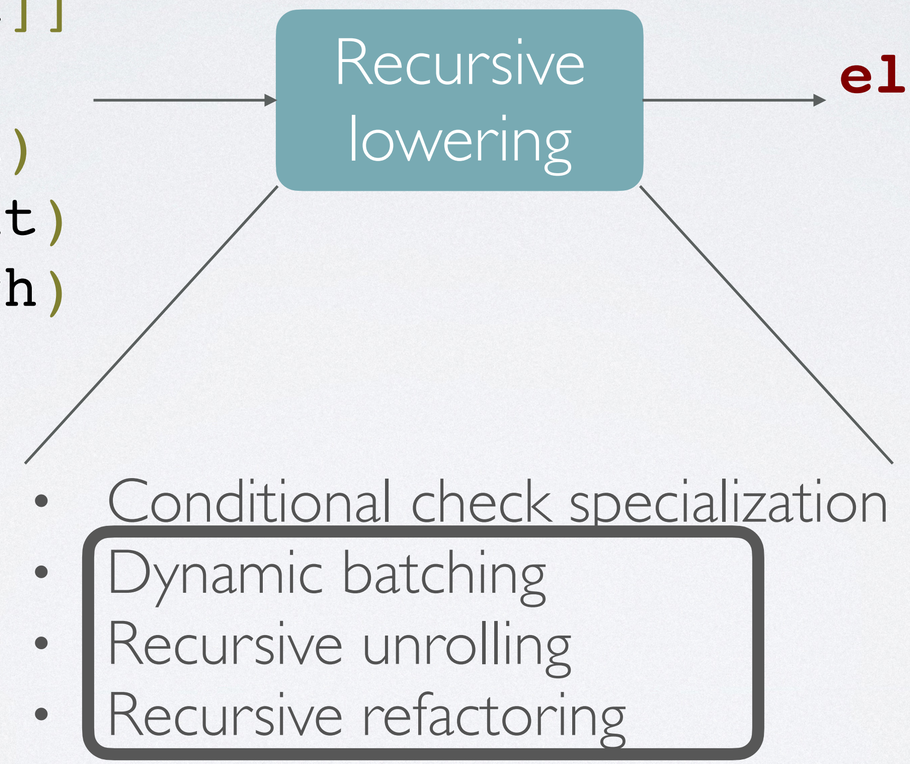


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Outline

- Motivation: Inefficiencies in Execution of Recursive Models
- Cortex: Our Compiler Based Solution
  - Recursive Scheduling
  - **Loop IR Lowering**
- Evaluation
- Conclusion

Loop IR Allows Tensor Compiler-Like Scheduling

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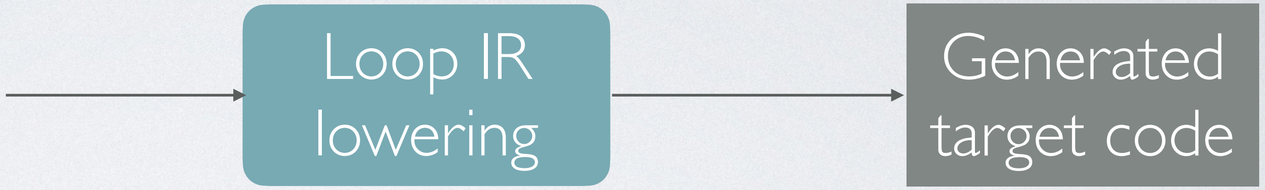

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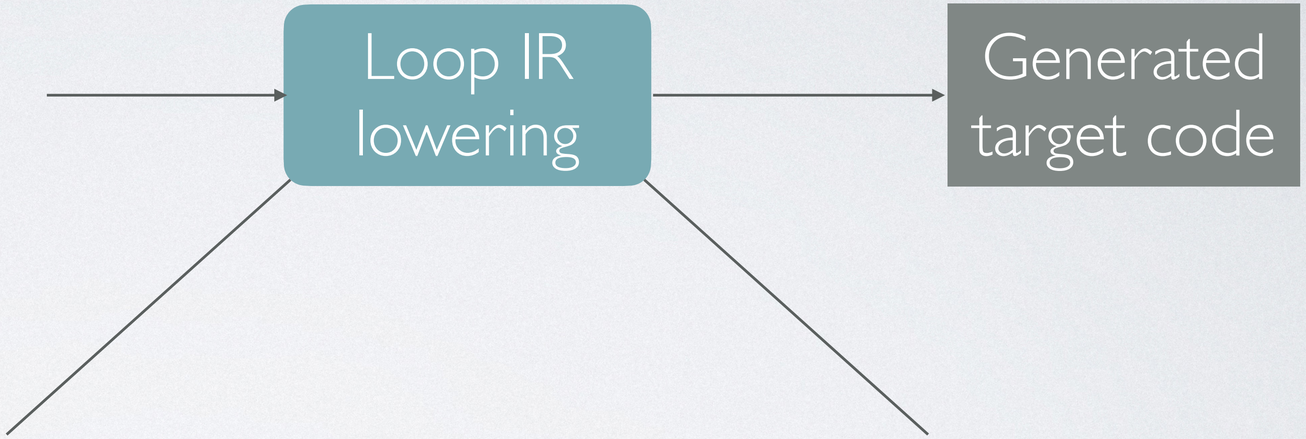

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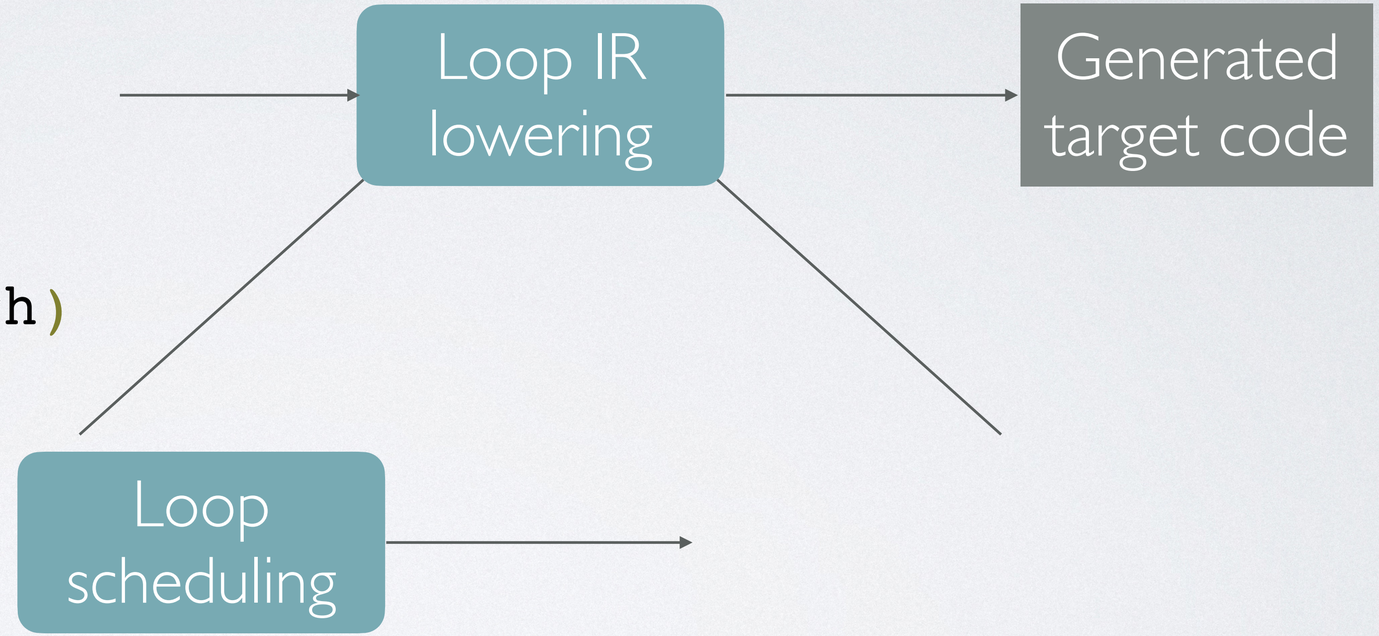

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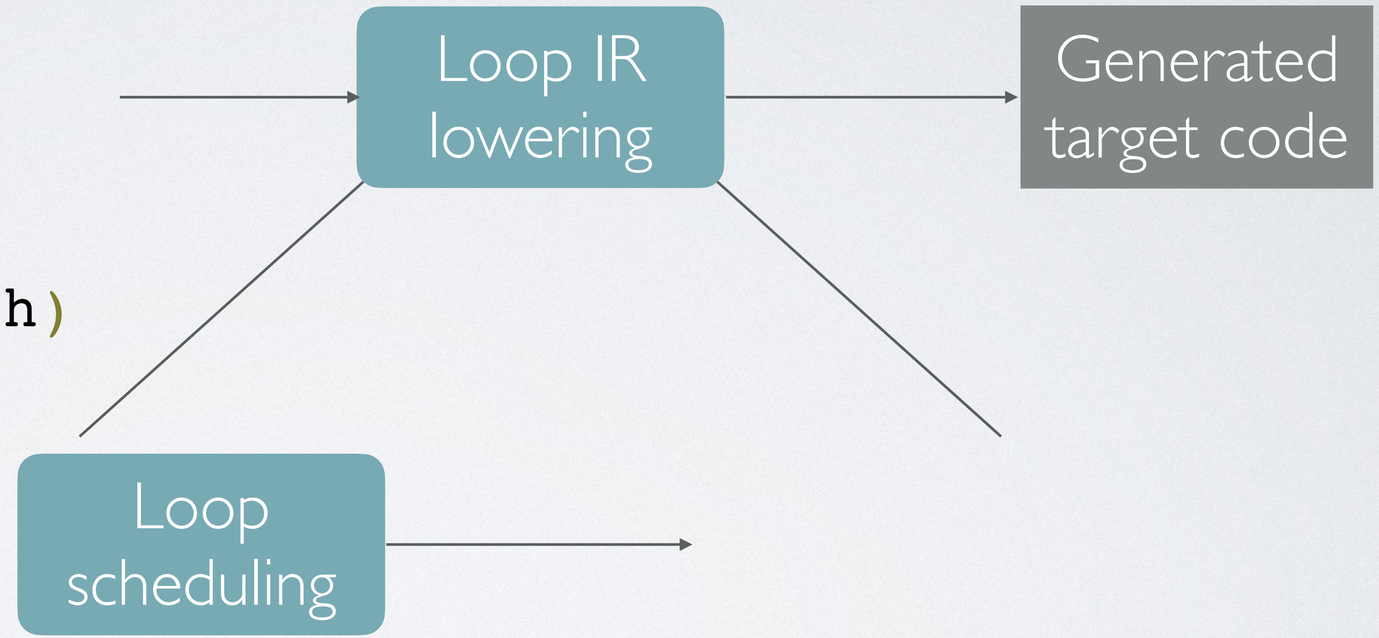

Scheduling primitives

- Loop tiling, unrolling, etc

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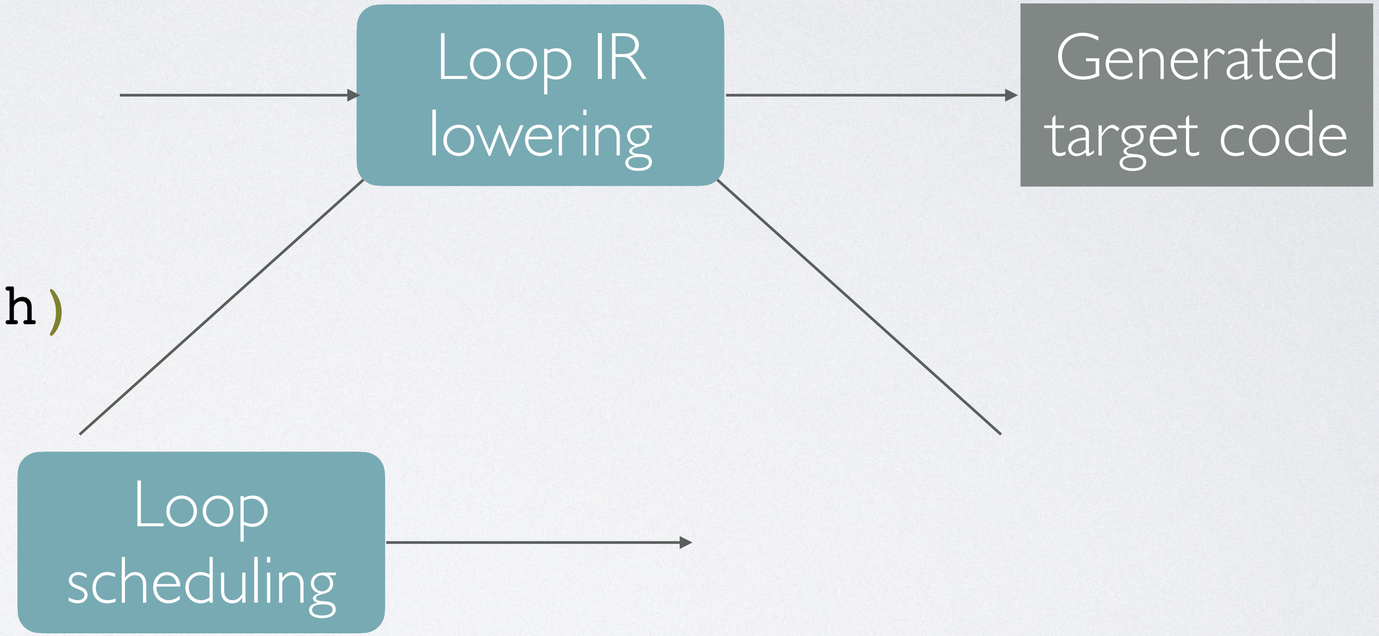

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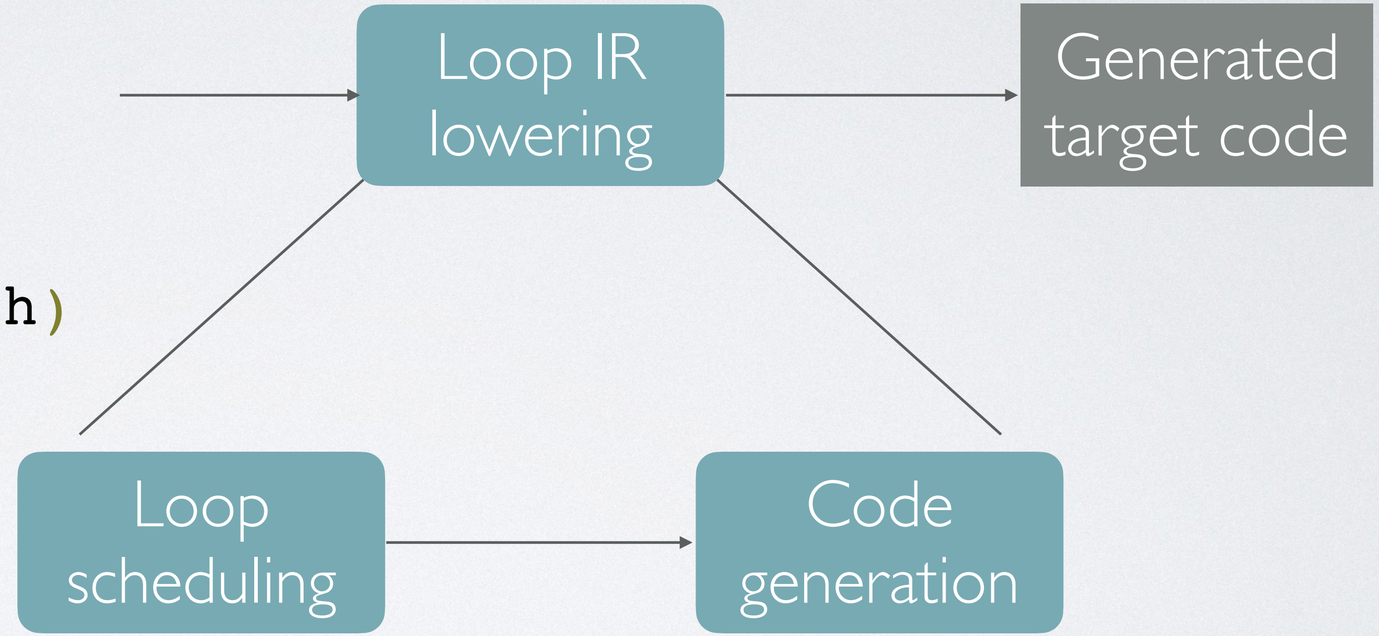

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Evaluation Setup

- Inference latencies measured for PyTorch, DyNet, Cavs and Cortex

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Models	Dataset	Hidden Size
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TreeFC	Synthetic perfect binary trees of height 10	256
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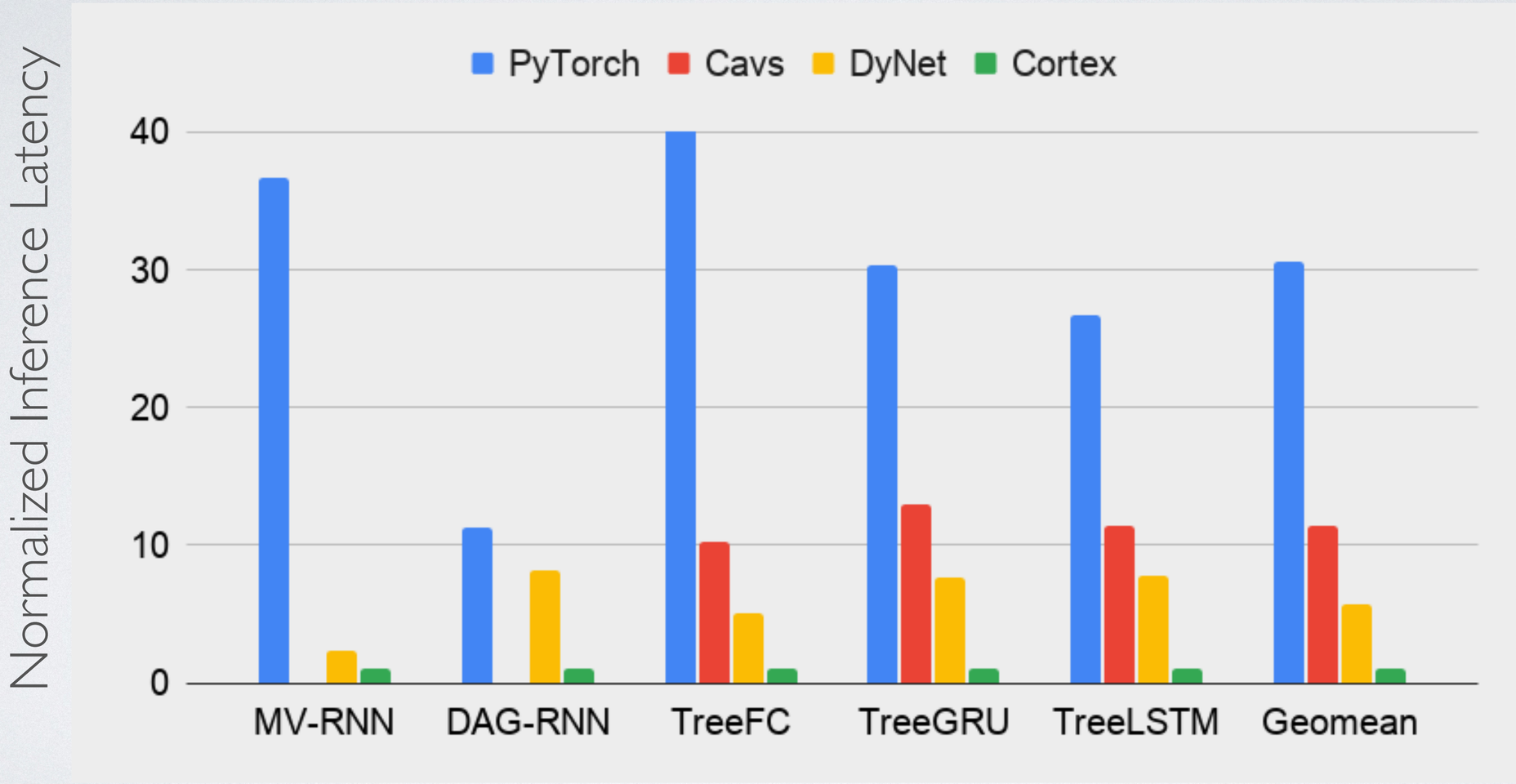
Inference Latencies on Nvidia V100 GPU

Lower is better



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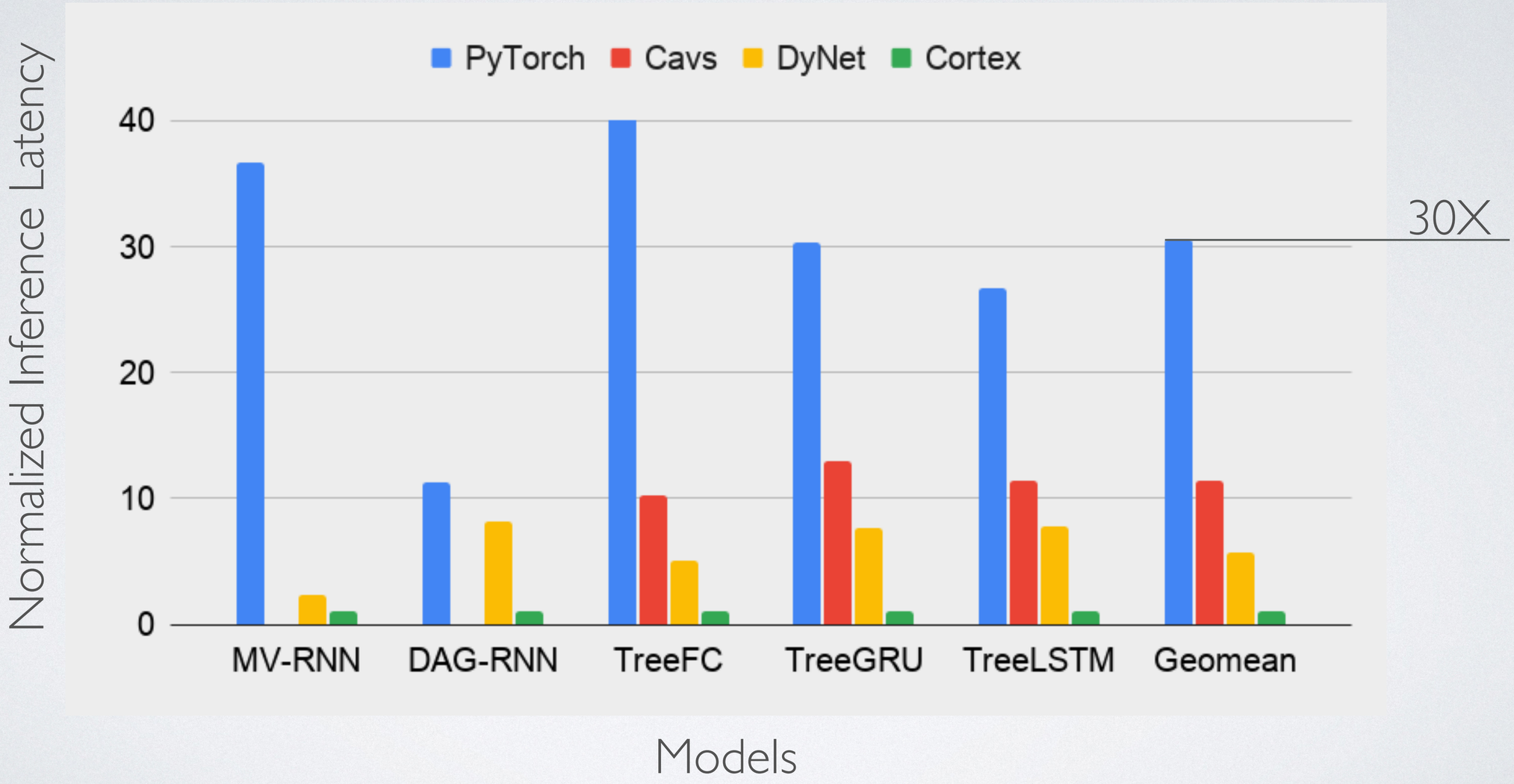

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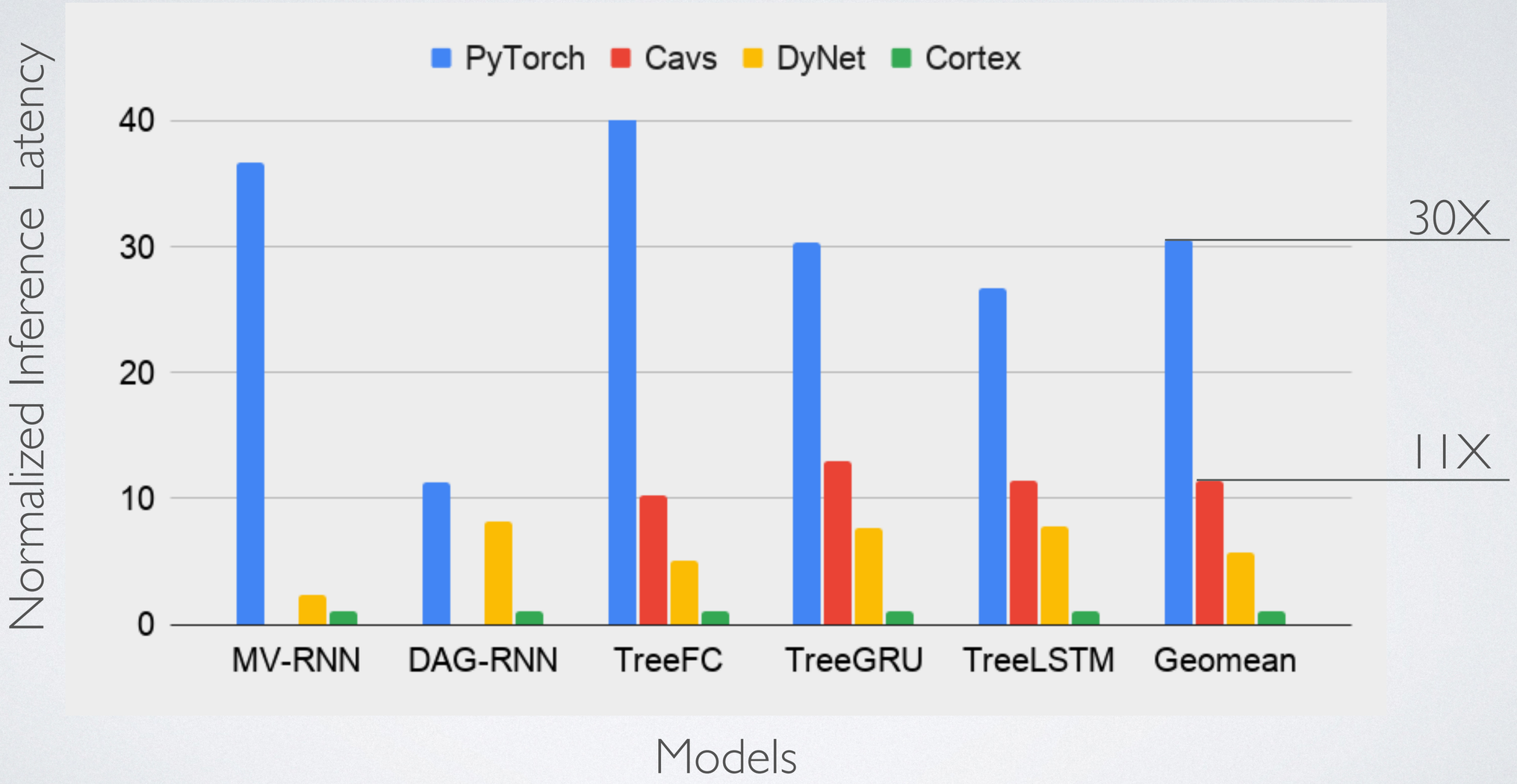

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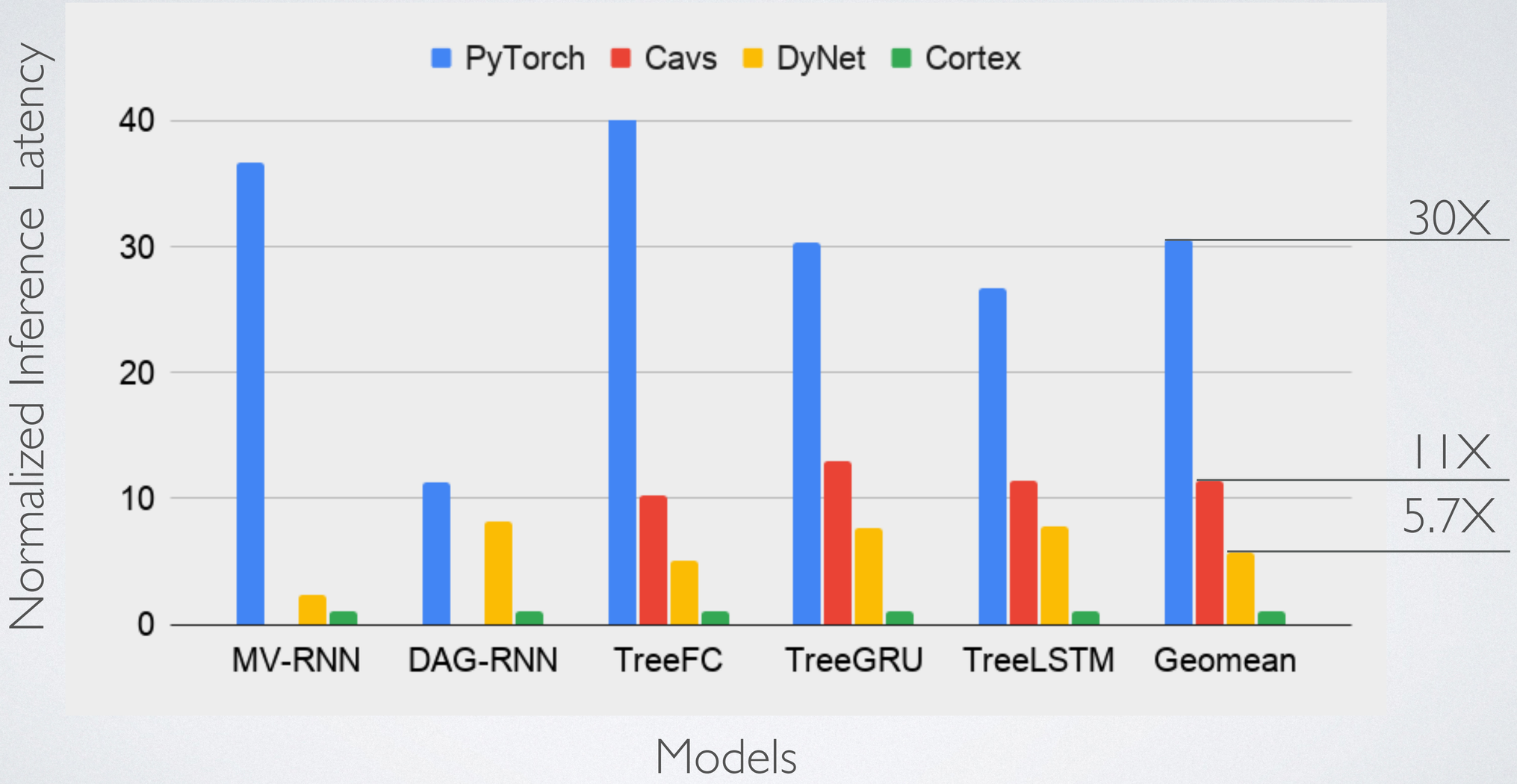

Inference Latencies for TreeLSTM Model

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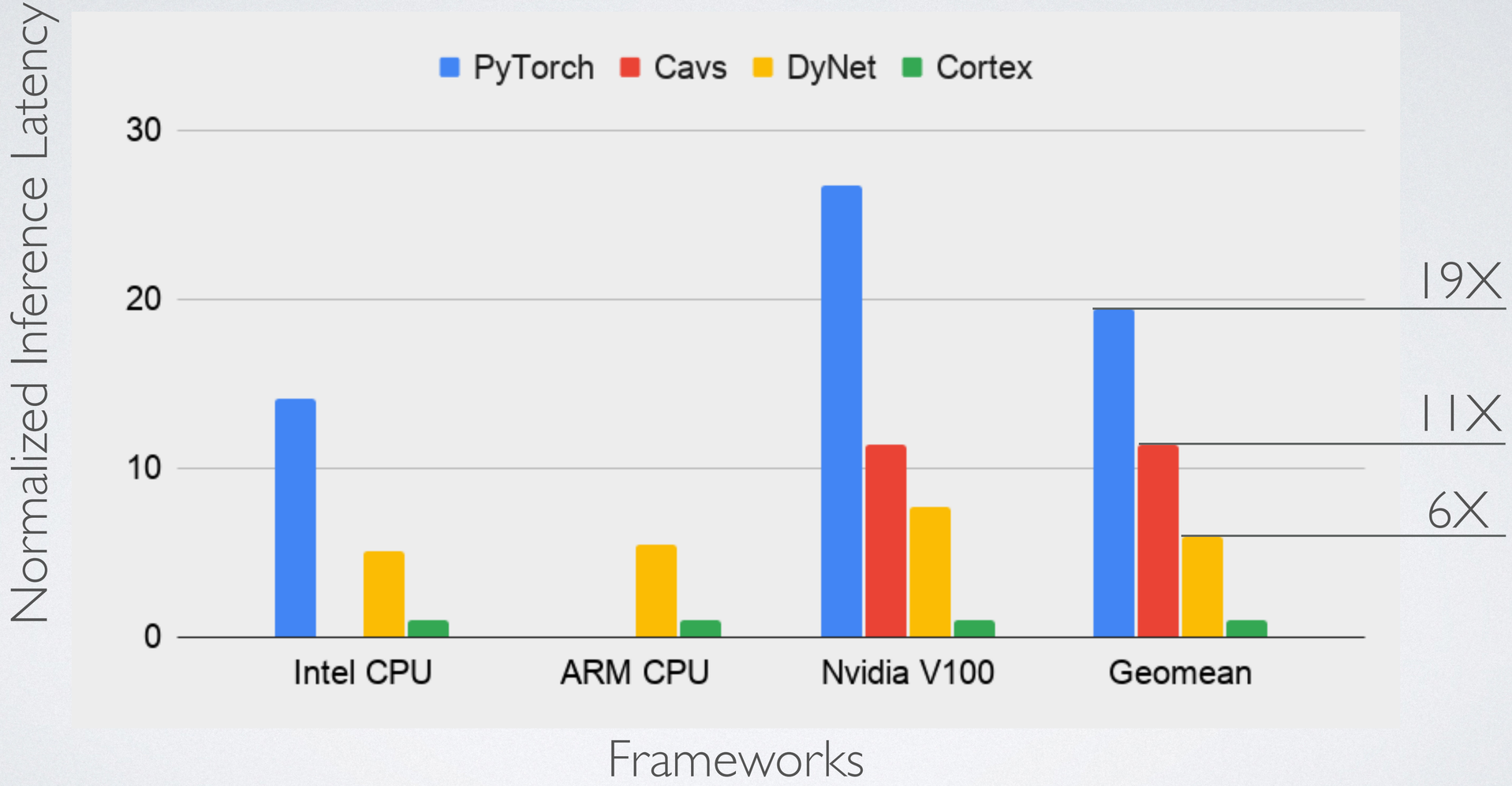

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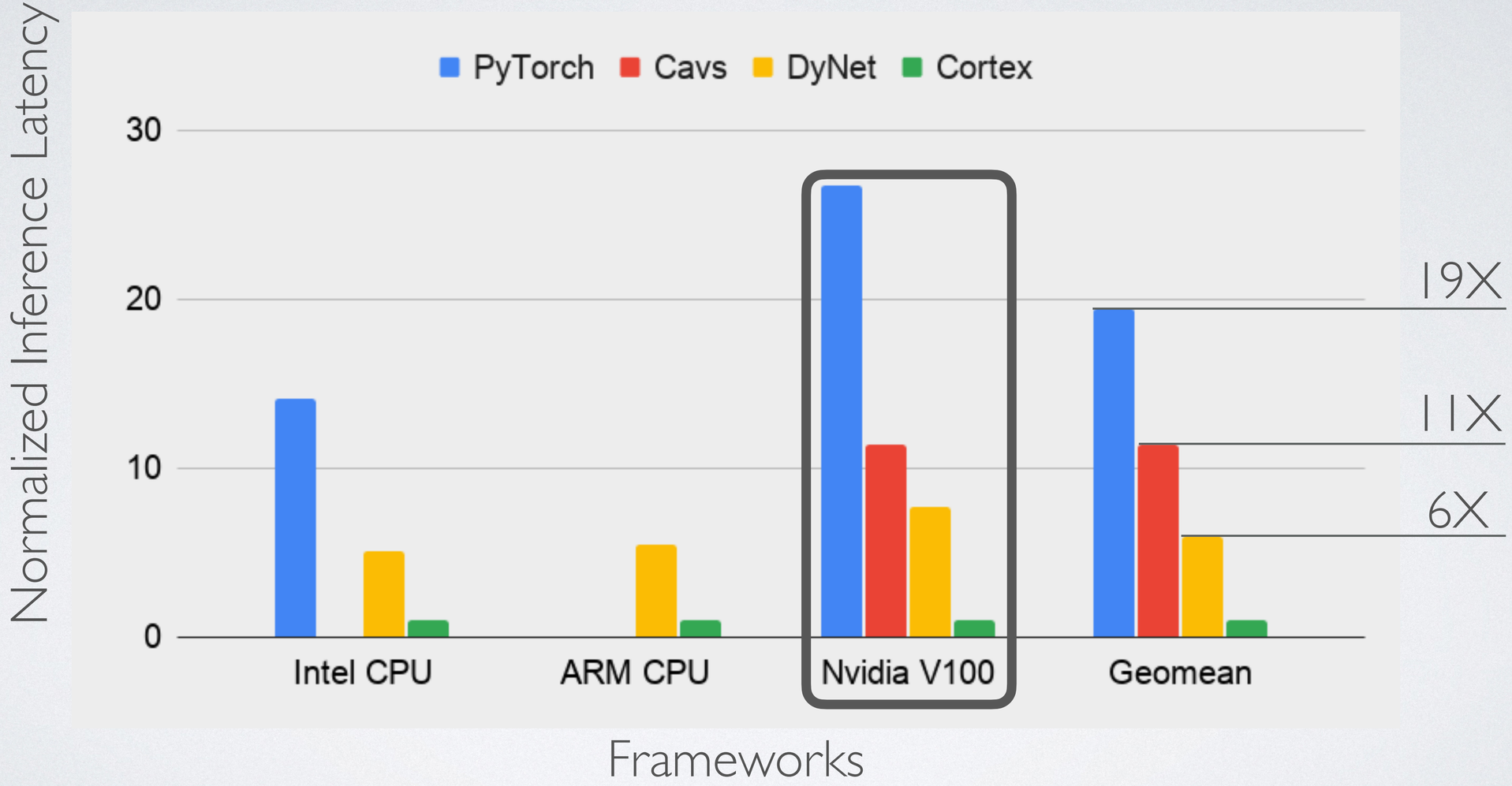

Cortex Has Low Scheduling Overheads

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Framework	#Kernel calls
DyNet	389
Cavs	122
Cortex	1

Cortex Has Low Scheduling Overheads

Framework	#Kernel calls	Scheduling time (ms)
DyNet	389	3.03
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Cortex Has Low Scheduling Overheads

Framework	#Kernel calls	Scheduling time (ms)	Memory mgmt. time (ms)
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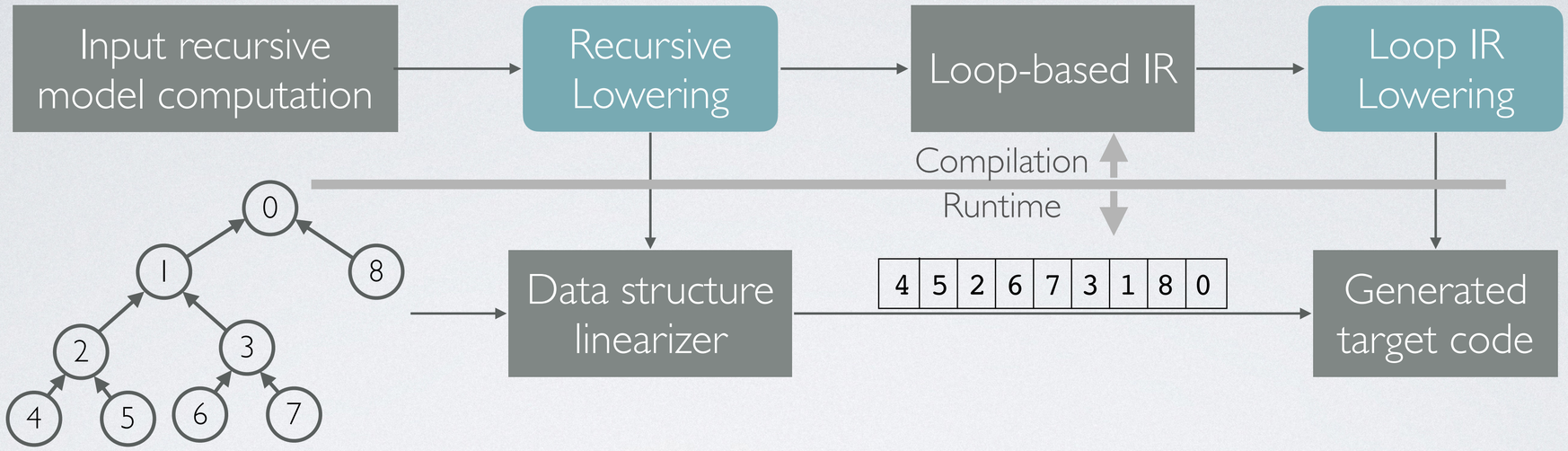
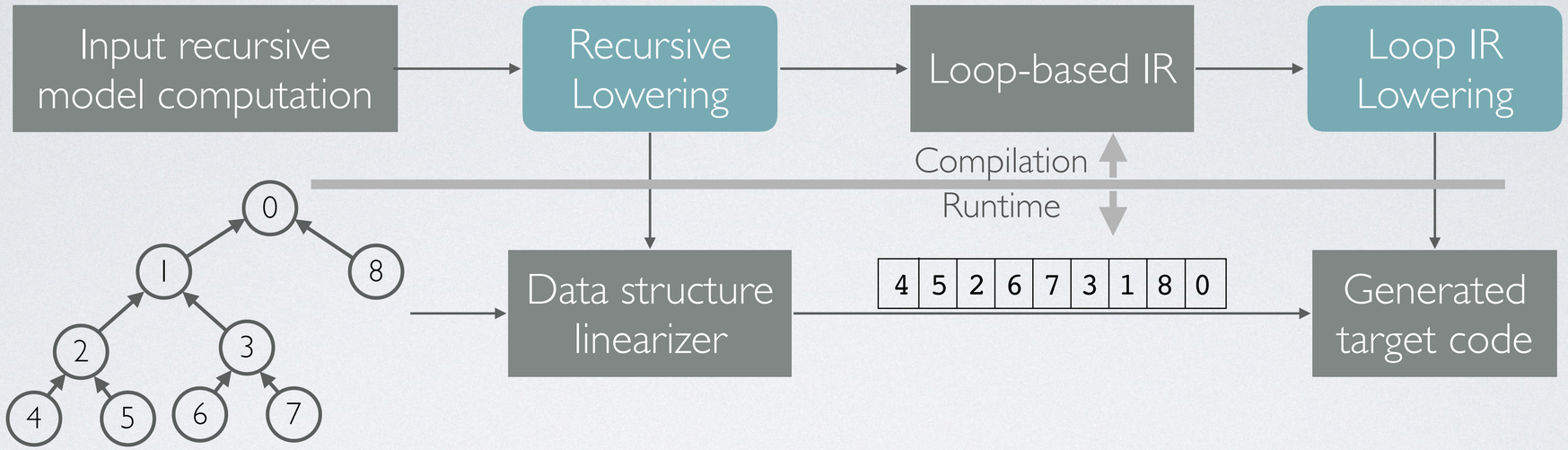
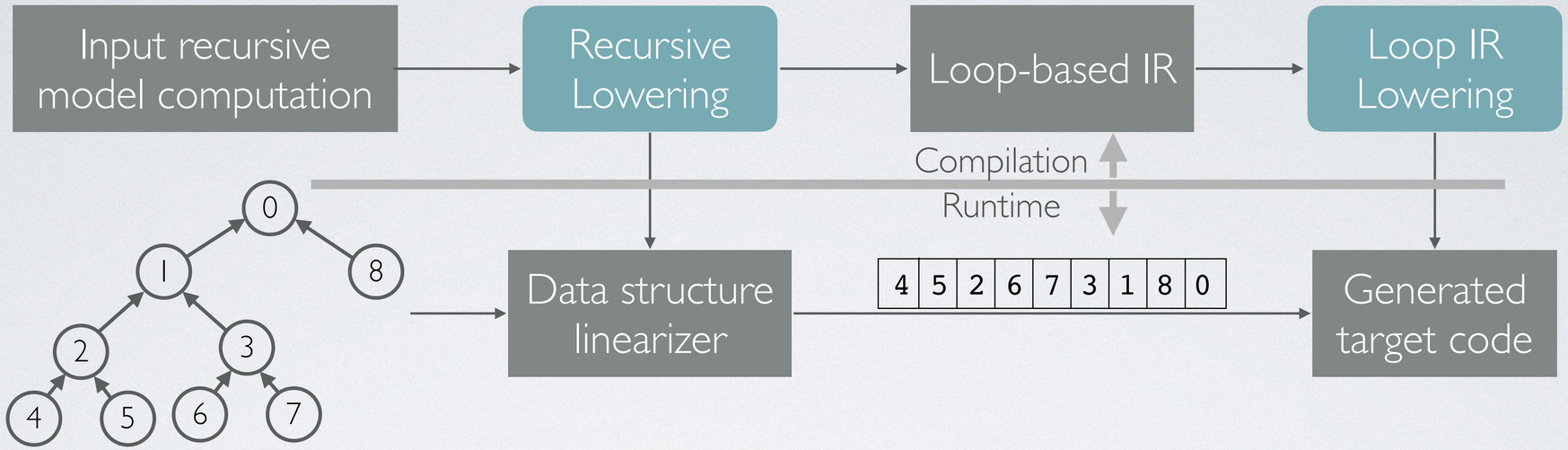

Input recursive model computation
Recursive Lowering
Loop-based IR
Loop IR Lowering
Compilation
Runtime
0
1
8
2
3
4
5
6
7
Data structure linearizer
4 5 2 6 7 3 1 8 0
Generated target code

Conclusion



- Linearizes recursive input structures to allow for efficient loop-based code generation

Conclusion



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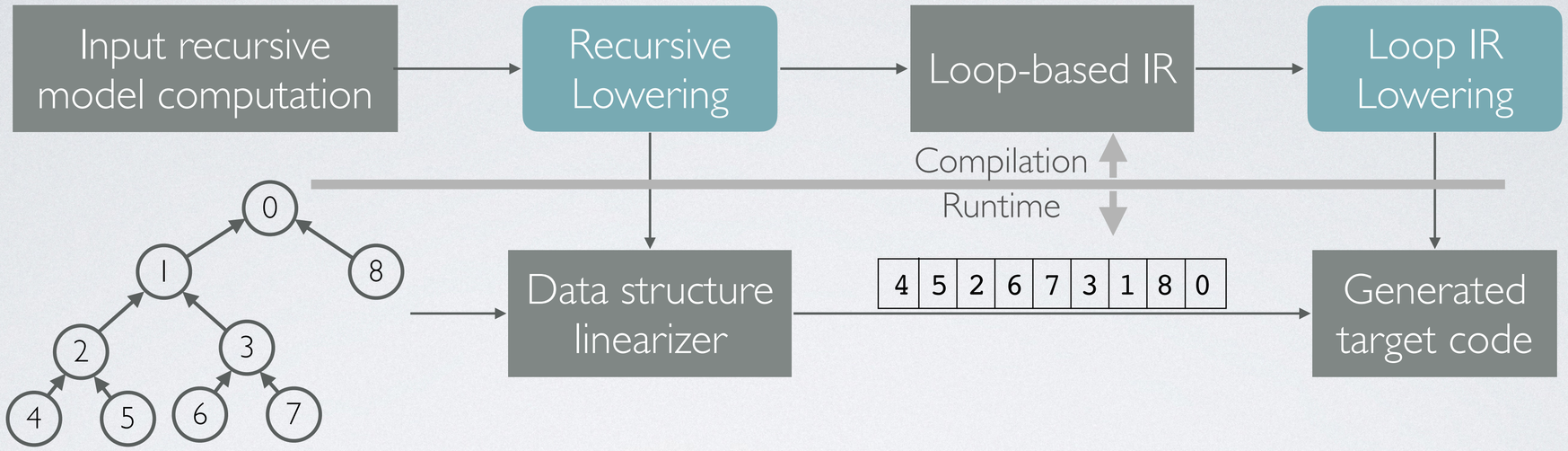

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- Enables end-to-end optimizations with low overheads
- Achieves up to 14X faster inference on CPUs as well as GPUs